

**Sterne Kessler
Goldstein Fox**
ATTORNEYS AT LAW

Robert Greene Sterne
Edward J. Kessler
Jorge A. Goldstein
David K.S. Cornwell
Robert W. Esmond
Tracy-Gene G. Durkin
Michele A. Cimbalà
Michael B. Ray
Robert E. Sokohl
Eric K. Steffe
Michael Q. Lee
Steven R. Ludwig
John M. Covert
Linda E. Alcorn
Robert C. Millonig
Lawrence B. Bugaisky
Donald J. Featherstone
Michael V. Messinger

Judith U. Kim
Timothy J. Shea, Jr.
Patrick E. Garrett
Jeffrey T. Helvey
Heidi L. Kraus
Albert L. Ferro*
Donald R. Banowitz
Peter A. Jackman
Teresa U. Medler
Jeffrey S. Weaver
Kendrick P. Patterson
Vincent L. Capuano
Eldora Ellison Floyd
Thomas C. Fiala
Brian J. Del Buono
Virgil Lee Beaton
Theodore A. Wood
Elizabeth J. Haanes

Joseph S. Ostroff
Frank R. Cottingham
Christine M. Lhullier
Rae Lynn P. Guest
George S. Bardmesser
Daniel A. Klein*
Jason D. Eisenberg
Michael D. Specht
Andrea J. Kamage
Tracy L. Muller*
LuAnne M. DeSantis
Ann E. Summerfield
Aric W. Ledford*
Helene C. Carlson
Timothy A. Doyle*
Gaby L. Longworth
Lori A. Gordon*
Nicole D. Dretar*

Ted J. Ebersole
Jyoti C. Iyer*
Laura A. Vogel

Registered Patent Agents*
Karen R. Markowicz
Nancy J. Leith
Matthew J. Dowd
Aaron L. Schwartz
Katrina Yujian Pei Quach
Bryan L. Skelton
Robert A. Schwartzman
Teresa A. Colella
Jeffrey S. Lundgren
Victoria S. Rutherford
Michelle K. Holoubek
Robert H. DeSelms
Simon J. Elliott

Julie A. Heider
Mita Mukherjee
Scott M. Woodhouse
Michael G. Penn
Christopher J. Walsh

Of Counsel
Kenneth C. Bass III
Evan R. Smith
Marvin C. Guthrie

*Admitted only in Maryland
*Admitted only in Virginia
*Practice Limited to
Federal Agencies

December 14, 2004

WRITER'S DIRECT NUMBER:
(202) 772-8629

INTERNET ADDRESS:
DONF@SKGF.COM

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RECEIVED

DEC 20 2004

OFFICE OF PETITIONS

Mail Stop Petition

Re: U.S. Utility Patent Application
Application No. 09/662,832; Filed: September 15, 2000
For: **Alignment and Ordering of Vector Elements for Single Instruction
Multiple Data Processing**
Inventors: Van Hook *et al.*
Our Ref: 1778.0100002

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Petition for an Extension of Time Under 37 C.F.R. § 1.136(a)(1);
2. Fee Transmittal (PTO/SB/17);
3. Request for Reconsideration of Petition Under 37 C.F.R. § 1.47(a);
4. Statement of Facts in Support of Filing On Behalf of Non-Signing Inventor Under 37 C.F.R. § 1.47(a), including the following Exhibits:
 - A. Exhibit A, consisting of:
 - a. Copy of a letter sent to Timothy J. Van Hook on June 3, 2004;
 - b. Copy of a FedEx Shipping Label, showing the tracking number of the package sent to Timothy Van Hook on June 3, 2004;
 - c. Copy of a self-addresses stamped envelope as sent to Timothy J. Van Hook on June 3, 2004;
 - d. Copy of a Supplemental Declaration for Patent Application as sent to Timothy J. Van Hook on June 3, 2004;

**RECEIVED
MAY 12 2005
OICE/JCWS**

- e. Copy of U.S. Utility Patent Appl. No. 09/662,832 as filed on September 15, 2000 and sent to Timothy J. Van Hook on June 3, 2004;
 - f. Copy of a Preliminary Amendment filed September 15, 2000, as sent to Timothy J. Van Hook on June 3, 2004;
 - g. Copy of a Second Preliminary Amendment filed April 9, 2001, as sent to Timothy J. Van Hook on June 3, 2004;
 - h. Copy of an Amendment and Reply Under 37 C.F.R. § 1.111 filed January 24, 2002, as sent to Timothy J. Van Hook on June 3, 2004; and
 - i. Copy of a Preliminary Amendment Under 37 C.F.R. §1.114 filed May 22, 2002, as sent to Timothy J. Van Hook on June 3, 2004;
- B. Exhibit B, consisting of an email from FedEx dated June 4, 2004, confirming delivery of the FedEx Shipment to Timothy J. Van Hook on June 4, 2004;
- C. Exhibit C, consisting of:
- a. Copy of a letter sent to Timothy J. Van Hook on September 22, 2004;
 - b. Copy of a FedEx Shipping Label, showing the tracking number of the package sent to Timothy J. Van Hook on September 22, 2004;
 - c. Copy of a letter sent to Peter Yan-Tek Hsu on September 22, 2004;
 - d. Copy of a FedEx Shipping Label, showing the tracking number of the package sent to Peter Yan-Tek Hsu on September 22, 2004;
 - e. Copy of a letter sent to William A. Huffman on September 22, 2004;
 - f. Copy of a FedEx Shipping Label, showing the tracking number of the package sent to William A. Huffman on September 22, 2004;

- g. Copy of a letter sent to Henry P. Moreton on September 22, 2004;
- h. Copy of a FedEx Shipping Label, showing the tracking number of the package sent to Henry P. Moreton on September 22, 2004;
- i. Copy of a letter sent to Earl A. Killian on September 22, 2004;
- j. Copy of a FedEx Shipping Label, showing the tracking number of the package sent to Earl A. Killian on September 22, 2004;
- k. Copy of U.S. Utility Patent Appl. No. 09/662,832 as filed on September 15, 2000, and sent to the inventors on September 22, 2004;
- l. Copy of U.S. Utility Patent No. 5,933,650, issued August 3, 1999, as sent to the inventors on September 22, 2004;
- m. Copy of U.S. Utility Patent No. 6,266,758 B1, issued July 24, 2001, as sent to the inventors on September 22, 2004;
- n. Copy of a list of allowed claims for U.S. Utility Application No. 09/662,832, filed September 15, 2000, as sent to the inventors on September 22, 2004;
- o. Copy of an original executed Declaration and Power of Attorney for a Patent Application as filed in grandparent U.S. Utility Patent Application No. 08/947,649 on July 16, 1998 (in five parts), as sent to the inventors on September 22, 2004;
- p. Copy of a Declaration for Patent Application for U.S. Utility Patent No. 5,933,650, issued August 3, 1999, as sent to the inventors on September 22, 2004;
- q. Copy of a Declaration for Patent Application for U.S. Utility Patent No. 6,266,758 B1, issued July 24, 2001, as sent to the inventors on September 22, 2004;
- r. Copy of a Declaration for Patent Application for U.S. Utility Application No. 09/662,832, filed September 15, 2000, as sent to the inventors on September 22, 2004; and

- s. Copy of 37 C.F.R. 10.18(b) and (c): Effect of Signature and Certificate for Correspondence Filed in the Patent and Trademark Office as sent to the inventors on September, 22, 2004;
- D. Exhibit D, consisting of an email from FedEx dated September 23, 2004, confirming delivery of the FedEx Shipment to Henry P. Moreton on September 23, 2004;
- E. Exhibit E, consisting of an email from FedEx dated September 23, 2004, confirming delivery of the FedEx Shipment to Timothy J. Van Hook on September 23, 2004;
- F. Exhibit F, consisting of an email from FedEx dated September 23, 2004, confirming delivery of the FedEx Shipment to William A. Huffman on September 23, 2004;
- G. Exhibit G, consisting of an email from FedEx dated September 23, 2004, confirming delivery of the FedEx Shipment to Earl A. Killian on September 23, 2004;
- H. Exhibit H, consisting of an email from FedEx dated September 23, 2004, confirming delivery of the FedEx Shipment to Peter Yan-Tek Hsu on September 27, 2004;
- I. Exhibit I, consisting of an email sent by LuAnne M. DeSantis, Esq. to Peter Yan-Tek Hsu on October 20, 2004;
- J. Exhibit J, consisting of an email sent by LuAnne M. DeSantis, Esq. to Peter Yan-Tek Hsu on November 30, 2004;
- K. Exhibit K, consisting of an email sent by LuAnne M. DeSantis, Esq. to William A. Huffman on October 20, 2004;
- L. Exhibit L, consisting of an email sent by LuAnne M. DeSantis, Esq. to Williams A. Huffman on November 30, 2004;
- M. Exhibit M, consisting of a letter sent by William A. Huffman to Donald J. Featherstone dated December 7, 2004;
- N. Exhibit N, consisting of an email sent by LuAnne M. DeSantis, Esq. to Earl A. Killian on October 25, 2004;

- O. Exhibit O, consisting of an email sent by LuAnne M. DeSantis, Esq. to Earl A. Killian on November 30, 2004; and
- P. Exhibit P, consisting of an email sent by Earl A. Killian to LuAnne M. DeSantis, Esq. on December 1, 2004;
- 5. Copy of an original Declaration for Patent Application executed by Henry P. Moreton;
- 6. Credit Card Payment Form (PTO-2038) for \$2360.00 to cover:
 - \$2160.00 Extension of Time Under 37 C.F.R. § 1.136(a)(1); and
 - \$ 200.00 Petition Fee Under 37 C.F.R. § 1.17(g); and
- 7. One (1) return postcard.


It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that additional extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

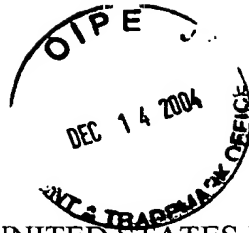
for:


Donald J. Featherstone
Attorney for Applicants
Registration No. 33,876

Reg. No. 33,997

DJF/LMY:krd
Enclosures

343111_1.DOC



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Van Hook *et al.*

Appl. No.: 09/662,832

Filed: September 15, 2000

For: **Alignment and Ordering of Vector
Elements for Single Instruction
Multiple Data Processing**

Confirmation No.: 2552

Art Unit: 2183

Examiner: Pan, Daniel H.

Atty. Docket: 1778.0100002

RECEIVED

DEC 20 2004

**Statement Of Facts In Support of Filing On Behalf Of Non-Signing
Inventors Under 37 C.F.R. § 1.47(a)**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Mail Stop Petition

Sir:

I, LuAnne M. DeSantis, Esq., hereby declare:

1. I am making this statement of facts in support of filing on behalf of non-signing inventors under 37 C.F.R. § 1.47(a) with regard to U.S. Non-Provisional Patent Application No. 09/662,832, filed September 15, 2000 ("the '832 patent application").

2. I am employed at the law firm of Sterne, Kessler, Goldstein & Fox P.L.L.C. ("SKGF"), 1100 New York Avenue, N.W., Washington, D.C. 20005-3934.

3. Mr. Timothy J. Van Hook ("Mr. Van Hook") is an inventor named in the '832 patent application. His last known address as of September 23, 2004, is as follows:

224 Oakgrove Avenue
Atherton, CA 94027

4. Mr. Peter Yan-Tek Hsu ("Mr. Hsu") is an inventor named in the '832 patent application. His last known address as of September 27, 2004, is as follows:

1 Rausch Street, Unit F
San Francisco, CA 94103

12/15/2004 CNGUYEN 00000064 09662832 200.00 DP
02 FC:1463

5. Mr. William A. Huffman ("Mr. Huffman") is an inventor named in the '832 patent application. His last known address as of September 23, 2004, is as follows:

16205 Roseleaf Lane
Los Gatos, CA 95032

6. Mr. Earl A. Killian ("Mr. Killian") is an inventor named in the '832 patent application. His last known address as of September 23, 2004, is as follows:

27961 Central Drive
Los Altos Hills, CA 94022

7. The invention(s) disclosed and/or claimed in the above-identified patent application were made while Mr. Van Hook, Mr. Hsu, Mr. Huffman, and Mr. Killian (collectively, "the non-signing inventors") were employed by Silicon Graphics, Inc. ("SGI"), 2011 N. Shoreline Boulevard, Mountain View, California, 94043-1389. The '832 patent application is now assigned to MIPS Technologies, Inc. ("MIPS"). The non-signing inventors are not currently employed at either SGI or MIPS.

8. The '832 patent application is a continuation of U.S. Non-Provisional Patent Application No. 09/263,798 ("the '798 patent application"), filed March 5, 1999 (now U.S. Patent No. 6,266,758), which is a continuation of U.S. Non-Provisional Patent Application No. 08/947,649 ("the '649 patent application"), filed October 9, 1997 (now U.S. Pat. No. 5,933,650).

9. According to SKGF records, a Declaration was signed for the '649 patent application by all inventors except for Mr. Van Hook. The attorney that filed the application, James P. Hao, Esq., signed the Declaration in place of Mr. Van Hook and mistakenly filed it under 37 C.F.R. § 1.47(b) in response to a Notice to File Missing Parts of Application (on

July 16, 1998). The Declaration was filed along with its fee, a Petition Form for Signature by Person with Sufficient Proprietary Interest on Behalf of Omitted Inventor(s) Who Refuse(s) to Sign or Cannot Be Reached (37 CFR 1.47(b)) and a Statement of Facts in Support of Filing on Behalf of Nonsigning Inventor Under 37 C.F.R. § 1.47(b). Responsibility, as well as the physical files, for the '649, the '798, and the '832 patent applications were subsequently transferred to SKGF. According to SKGF records, no decision was ever received from the USPTO. (Also note that an unsigned Supplemental Declaration and Power of Attorney for a Patent Application was subsequently filed in the '649 patent application on January 6, 1999, to show the citizenship of all inventors as required in an Office Action dated October 9, 1998.)

10. According to SKGF records, the '798 patent application, which claims priority to the '649 patent application, was filed with the Declaration that was filed in the '649 patent application on July 16, 1998. This Declaration was also filed with the Petition Form and Statement of Facts that was filed in the '649 patent application. According to SKGF records, no decision was ever received from the USPTO.

11. According to SKGF records, the '832 patent application was filed with the Declaration that was filed in the '649 patent application on July 16, 1998. The Declaration issue was discovered when reviewing the '832 patent application file in preparation for paying the Issue Fee.

12. During the period of April 15 through May 20, 2004, SKGF made multiple telephone calls to the Office of Petitions in attempts to get guidance on what action should be taken to correct any deficiencies in the originally filed Declaration in the '832 application and

in a similarly situated, commonly owned application. We initially sought to obtain only the Declaration signature of Mr. Van Hook. However, during a telephone call on June 15, 2004, Ms. Alesia M. Brown of the Office of Petitions recommended that a new Declaration be executed by all inventors listed on the '832 application. Our first attempts to get only Mr. Van Hook's signature and our subsequent attempts to get signatures from all inventors are detailed in the following paragraphs.

13. On the evening of June 2, 2004, I spoke with Mr. Van Hook via telephone. I explained the situation and asked if I could verify his mailing address. He verified that his mailing address was as indicated above in paragraph number 3. Mr. Van Hook stated that, due to the history between his former employer and himself, he may or may not open any package sent to him on behalf of our client, and that he may or may not sign or return anything. He explained, in some detail, that a lawsuit related to intellectual property and/or trade secrets had been brought against him in the past by his former employer. The lawsuit had since been dropped. However, Mr. Van Hook stated that he would not sign anything without a release stating that suit will never be brought against him again.

14. On June 3, 2004, SKGF sent a package via Federal Express to Mr. Van Hook that included a letter signed by Mr. Donald J. Featherstone, Esq. of SKGF, a copy of the '832 patent application, copies of subsequent amendments made to the '832 patent application, and a Supplemental Declaration (see EXHIBIT A).

15. On June 4, 2004, SKGF received email confirmation from Federal Express that the package sent on June 3, 2004, to Mr. Van Hook was received and signed for by

".VANHOOK." (see EXHIBIT B). No response to the package was ever received from Mr. Van Hook.

16. On September 1, 2004, I left a voicemail message for Mr. Henry P. Moreton ("Mr. Moreton," a co-inventor), briefly explaining the situation and asking for a return call. No return call was received.

17. On September 1, 2004, I spoke with Mr. Hsu via telephone and briefly explained the situation. Mr. Hsu verified that his current mailing address was as indicated above in paragraph number 4. On September 2, 2004, I emailed Mr. Hsu to verify his correct full name. He responded via email the same day with an explanation of his full name.

18. On September 1, 2004, I left a voicemail message for Mr. Huffman, briefly explaining the situation and asking for a return call. On September 2, 2004, I received an email from Jeannette Schreckenghaust at SGI (Mr. Huffman's former employer), forwarding an email from Mr. Huffman asking if she was aware of the situation and asking if she was familiar with the requesting law firm (SKGF). On September 9, 2004, Mr. Huffman telephoned me and verified that his current mailing address was as indicated above in paragraph number 5.

19. On September 1, 2004, I left a voicemail message for Mr. Killian, briefly explaining the situation and asking for a return call. No return call was received.

20. On September 22, 2004, SKGF sent a package via Federal Express to all of the inventors (Mr. Van Hook, Mr. Hsu, Mr. Huffman, Mr. Killian, and Mr. Moreton). The package included a letter signed by Mr. Donald J. Featherstone, Esq. of SKGF, copies of the

'758 and '650 patents, a copy of the '832 patent application and currently allowed claims, a copy of the original Declaration from the '649 patent application, three new Declarations (one for each of the '649, '798, and '832 patent applications), and a copy of 37 C.F.R. § 10.18(b) and (c) (see EXHIBIT C).

21. On September 23, 2004, SKGF received emails from Federal Express confirming that the packages sent on September 22, 2004, were delivered to Mr. Moreton (signed for by "K.GREEN.", see EXHIBIT D), Mr. Van Hook (signed for by ".VANHOOK.", see EXHIBIT E), Mr. Huffman (signed for by "W..HUFFMAN.", see EXHIBIT F), and Mr. Killian (signed for by "L.EE.", see EXHIBIT G).

22. On September 27, 2004, SKGF received email confirmation from Federal Express that the package sent on September 22, 2004, was delivered to Mr. Hsu (signed for by "J.TRACY.", see EXHIBIT H).

23. On October 7, 2004, newly executed Declarations were received from Mr. Moreton.

24. On October 20, 2004, I sent a follow-up email to Mr. Hsu (see EXHIBIT I). No response was received. On October 29, 2004, I left a voicemail message for Mr. Hsu asking him to return the call. No return call was received. On November 30, 2004, I sent another follow-up email (see EXHIBIT J) to Mr. Hsu that includes the statement, "If we do not receive a response from you by Monday, December 13, 2004, we will assume that you refuse to cooperate in prosecuting/maintaining the above-captioned patent application/patents." No response was received. I have not received any further communications from Mr. Hsu.

25. On October 20, 2004, I sent a follow-up email to Mr. Huffman (see EXHIBIT K). No response was received. On October 29, 2004, I telephoned Mr. Huffman and was asked by the female person who answered the telephone to call back in a few minutes because Mr. Huffman was indisposed. Upon returning the call, I was told by the same female person that he had since stepped out and that she would give him a message to call me. On October 30, 2004, Mr. Huffman left a message on my voicemail stating that he had not yet looked at the package and therefore had nothing to report to me at the time. On November 30, 2004, I sent another follow-up email to Mr. Huffman (see EXHIBIT L) that includes the statement, "If we do not receive a response from you by Monday, December 13, 2004, we will assume that you refuse to cooperate in prosecuting/maintaining the above-captioned patent application/patents." On December 10, 2004, a letter addressed to Donald J. Featherstone from William A. Huffman was received by SKGF (see EXHIBIT M), along with a newly executed Declaration for the grandparent application (the '649 patent application, now U.S. Patent No. 5,933,650). Mr. Huffman stated in his letter that he did not have time to review the '758 patent or '832 patent application and therefore would be "unable to assist you [SKGF] with the two additional declarations." I have not received any further communications from Mr. Huffman.

26. On October 25, 2004, I sent a follow-up email to Mr. Killian (see EXHIBIT N). No response was received. On October 29, 2004, I spoke with Mr. Killian via telephone and explained the situation briefly. I asked him if he had any questions regarding the package sent on September 22, 2004. Mr. Killian stated that he would consider looking at the package and would call back if he had any questions. He expressed hesitation signing or certifying anything that he had worked on such a long time ago in his career. On November

30, 2004, I sent another follow-up email to Mr. Killian (see EXHIBIT O) that includes the statement, "If we do not receive a response from you by Monday, December 13, 2004, we will assume that you refuse to cooperate in prosecuting/maintaining the above-captioned patent application/patents." Mr. Killian responded by email on December 1, 2004, indicating that he believes reviewing the documentation is not currently a good use of his time and that he will not be signing the Declarations (see EXHIBIT P). I have not received any further communications from Mr. Killian.

27. On October 29, 2004, I telephoned Mr. Van Hook and left a message asking if he had any questions regarding the package sent on September 22, 2004. He returned the call the same day. I explained the situation again briefly. He stated that he had received the package, but again refused to review or sign anything. I have not received any further communications from Mr. Van Hook.

I declare that all statements made herein of my own knowledge are true and that all statements made on information from review of the file history of the patent application are believed to be true, and further that these statements were made with the knowledge that willful false statements or the like so made are punishable by fine or imprisonment or both

Van Hook *et al.*
Appl. No. 09/662,832

under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the patent application or any patent issued thereon.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

A handwritten signature in cursive script, reading "LuAnne M. DeSantis".

LuAnne M. DeSantis

Date: 12/14/04

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

276187_1.DOC



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Van Hook *et al.*

Appl. No.: 09/662,832

Filed: September 15, 2000

For: **Alignment and Ordering of Vector
Elements for Single Instruction
Multiple Data Processing**

Confirmation No.: 2552

Art Unit: 2183

Examiner: Pan, Daniel H.

Atty. Docket: 1778.0100002

Petition for Extension of Time Under 37 C.F.R. § 1.136(a)(1)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

RECEIVED

DEC 20 2004

OFFICE OF PETITIONS

It is hereby requested that the period for replying to the Decision Refusing Status Under 37 C.F.R. § 1.47(a) be extended five months from July 14, 2004 to December 14, 2004 by the filing of this Petition and fee payment.

The petition fee set forth in 37 C.F.R. § 1.17(a) is believed to be \$2,160.00 for a five-month extension of time for a large entity. Fee payment is provided in our accompanying Credit Card Payment Form (PTO-2038). However, if extensions of time under 37 C.F.R. § 1.136 other than those provided herewith are required to prevent abandonment of the present patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,


STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

12/15/2004 CNGUYEN 00000064 09662832

01 FC:1255

2160.00 OP

for:

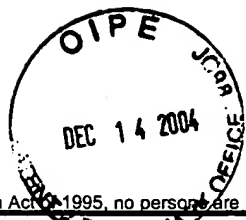

Donald J. Featherstone
Attorney for Applicants
Registration No. 33,876

Reg. No. 33,997

Date: 12/14/04

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

343178_1.DOC



RECEIVED

DEC 20 2004

PTO/SB/17 (10-04v2)

Approved for Release by NSA on 09-11-2013 pursuant to E.O. 13526

U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no person is required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL for FY 2005

Effective 10/01/2004. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT (\$) 2360.00

Complete if Known

Application Number	09/662,832
Filing Date	September 15, 2000
First Named Inventor	Timothy J. Van Hook
Examiner Name	Pan, Daniel H.
Art Unit	2183
Attorney Docket No.	1778.0100002

METHOD OF PAYMENT (check all that apply)☐ Check ☒ Credit card ☐ Money Order ☒ Other ☐ None****Charge any deficiencies or credit any overpayments in the fees to Deposit Acct. No. 19-0036.**Deposit Account Number
Deposit Account Name

19-0036

Sterne, Kessler, Goldstein & Fox P.L.L.C.

The Director is authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Credit any overpayments☐ Charge any additional fee(s) or any underpayment of fee(s)☐ Charge fee(s) indicated below, except for the filing fee to the above-identified deposit account.**FEE CALCULATION****1. BASIC FILING FEE**

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
1001 790	2001 395	Utility filing fee	
1002 350	2002 175	Design filing fee	
1003 550	2003 275	Plant filing fee	
1004 790	2004 395	Reissue filing fee	
1005 160	2005 80	Provisional filing fee	
SUBTOTAL (1)			(\$) 0.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

Total Claims	Extra Claims	Fee from below	Fee Paid
Independent	-20** =	X	
Multiple Dependent	-3** =	X	

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description
1202 18	2202 9	Claims in excess of 20
1201 88	2201 44	Independent claims in excess of 3
1203 300	2203 150	Multiple dependent claim, if not paid
1204 88	2204 44	** Reissue independent claims over original patent
1205 18	2205 9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) (\$) 0.00

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)**3. ADDITIONAL FEES**

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
1051 130	2051 65	Surcharge - late filing fee or oath	
1052 50	2052 25	Surcharge - late provisional filing fee or cover sheet	
1053 130	1053 130	Non-English specification	
1812 2,520	1812 2,520	For filing a request for ex parte reexamination	
1804 920*	1804 920*	Requesting publication of SIR prior to Examiner action	
1805 1,840*	1805 1,840*	Requesting publication of SIR after Examiner action	
1251 110	2251 55	Extension for reply within first month	
1252 430	2252 215	Extension for reply within second month	
1253 980	2253 490	Extension for reply within third month	
1254 1,530	2254 765	Extension for reply within fourth month	
1255 2,080	2255 1,040	Extension for reply within fifth month	2160.00
1401 340	2401 170	Notice of Appeal	
1402 340	2402 170	Filing a brief in support of an appeal	
1403 300	2403 150	Request for oral hearing	
1451 1,510	1451 1,510	Petition to institute a public use proceeding	
1452 110	2452 55	Petition to revive - unavoidable	
1453 1,370	2453 685	Petition to revive - unintentional	
1501 1,370	2501 685	Utility issue fee (or reissue)	
1502 490	2502 245	Design issue fee	
1503 660	2503 330	Plant issue fee	
1460 130	1460 130	Petitions to the Commissioner	200.00
1807 50	1807 50	Processing fee under 37 CFR 1.17(q)	
1806 180	1806 180	Submission of Information Disclosure Stmt	
8021 40	8021 40	Recording each patent assignment per property (times number of properties)	
1809 790	2809 395	Filing a submission after final rejection (37 CFR 1.129(a))	
1810 790	2810 395	For each additional invention to be examined (37 CFR 1.129(b))	
1801 790	2801 395	Request for Continued Examination (RCE)	
1802 900	1802 900	Request for expedited examination of a design application	

Other fee (specify)

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) (\$) 2360.00**SUBMITTED BY**

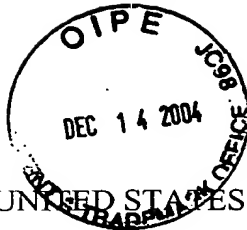
(Complete if applicable)

Name (Print/Type)	Donald J. Reatherstone	Registration No. (Attorney/Agent)	33,876	Telephone	(202) 371-2600
Signature	by: [Signature]	Reg. No.	33,997	Date	12/14/04

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Van Hook *et al.*

Appl. No.: 09/662,832

Filed: September 15, 2000

For: **Alignment and Ordering of Vector
Elements for Single Instruction
Multiple Data Processing**

Confirmation No.: 2552

Art Unit: 2183

Examiner: Pan, Daniel H.

Atty. Docket: 71100002

RECEIVED
DEC 20 2004
OFFICE OF PETITIONS

Request for Reconsideration of Petition Under 37 C.F.R. § 1.47(a)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Mail Stop Petition

Sir:

In response to the Decision Refusing Status Under 37 CFR 1.47(a) mailed **May 14, 2004**, and in accordance with the requirements of 37 C.F.R. § 1.47(a) and M.P.E.P. § 409.03(a), Petitioner has filed herewith the following documents:

- (1) An original Declaration for Patent Application executed by Henry P. Moreton, fulfilling the requirements of 37 C.F.R. § 1.47(a);
- (2) Statement of Facts in Support of Filing On Behalf of Non-Signing Inventors Under 37 C.F.R. § 1.47(a) from LuAnne M. DeSantis, Esq., along with referenced Exhibits A-P.

The Declaration for Patent Application has been signed by one of the five named joint inventors. Timothy J. Van Hook, Peter Yan-Tek Hsu, William A. Huffman, and Earl A. Killian have not executed the Declaration for Patent Application. Petitioner submits that the Declaration for Patent Application signed by Henry P. Moreton, with the signature blocks of the non-signing inventors left blank, should be considered as having been signed by all of the joint inventors on behalf of the non-signing inventors. *See* M.P.E.P. § 409.03(a)(A).

The Statement of Facts in Support of Filing on Behalf of Non-Signing Inventors Under 37 C.F.R. § 1.47(a), as required by M.P.E.P. § 409.03(a)(B), from LuAnne M. DeSantis, Esq., provides proof of the pertinent facts that the non-signing inventors refuse to sign. The Statement of Facts also indicates the last known addresses of the non-signing inventors as required by M.P.E.P. § 409.03(a)(C).

During the period April 15 through May 20, 2004, multiple telephone calls were made to the Office of Petitions in attempts to get guidance on what action should be taken to correct any deficiencies in the originally filed Declaration in the '832 application and in a similarly situated, commonly owned application. We initially sought to obtain only the Declaration signature of Mr. Timothy J. Van Hook, since he was the only non-signing inventor on the original Declaration filed in the grandparent application (U.S. Pat. Appl. No. 08/947,649, now U.S. Pat. No. 5,933,650). However, during a telephone call on June 15, 2004, Ms. Alesia M. Brown of the Office of Petitions stated that because the original Declaration filed in the grandparent application was executed improperly and because there is no indication that Rule 47 status was ever granted in the grandparent application, she recommended that a new Declaration be executed by *all* inventors listed on the '832 application. Our first attempts to get only Mr. Van Hook's signature and our subsequent attempts to get signatures from all inventors are detailed in the accompanying Statement of Facts.

Petitioner therefore respectfully submits that the documents filed herewith satisfy all the requirements of 37 C.F.R. § 1.47(a) and M.P.E.P. §§ 409.03(a), (d), and (e). Accordingly, Petitioner respectfully requests that the present application be accorded status under 37 C.F.R. § 1.47(a).

Van Hook *et al.*
Appl. No. 09/662,832

Payment of the fee for filing a petition under 37 C.F.R. § 1.47 set forth in 37 C.F.R. § 1.17(g) is provided in the accompanying Credit Card Payment Form (PTO-2038).

A Petition Under 37 C.F.R. § 1.136(a)(1) for a five-month extension of time accompanies this request. It is believed that no additional extension of time is necessary. However, if an additional extension of time is required to prevent abandonment of the present application, then such extension is hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



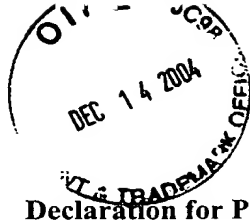
Reg. No. 33,997

for:

Donald J. Featherstone
Attorney for Applicants
Registration No. 33,876

Date: 12/14/04

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600



Declaration for Patent Application

RECEIVED

DEC 20 2004 Docket Number: 1778.0100002

As a below named inventor, I hereby declare that:

OFFICE OF PETITIONS

My residence, mailing address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter that is claimed and for which a patent is sought on the invention entitled **Alignment and Ordering of Vector Elements for Single Instruction Multiple Data Processing**, the specification of which is attached hereto unless the following box is checked:

- ☒ was filed on September 15, 2000;
as United States Application Number 09/662,832; and
was amended on September 15, 2000; April 9, 2001; January 24, 2002; May 22, 2002; and June 18, 2004.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or (f) or § 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or § 365(a) of any PCT international application, which designated at least one country other than the United States of America, listed below, and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Applications(s):

Priority Claimed

_____ (Application No.)	_____ (Country)	_____ (Day/Month/Year Filed)
_____ (Application No.)	_____ (Country)	_____ (Day/Month/Year Filed)

☐ Yes ☐ No

☐ Yes ☐ No

Send Correspondence to:

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 New York Avenue, N.W.
Washington, D.C. 20005-3934

Direct Telephone Calls to:

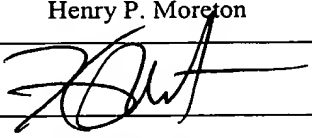
(202) 371-2600

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first Inventor:	Timothy J. Van Hook
Signature of first Inventor:	Date:
Residence:	Atherton, CA
Citizenship:	U.S.A.
Mailing Address:	224 Oakgrove Avenue Atherton, CA, 94027

Full name of second Inventor:	Peter Yan-Tek Hsu
Signature of second Inventor:	Date:
Residence:	San Francisco, CA
Citizenship:	U.S.A.
Mailing Address:	1 Rausch Street, Unit F San Francisco, CA, 94103

Full name of third Inventor:	William A. Huffman
Signature of third Inventor:	Date:
Residence:	Los Gatos, CA
Citizenship:	U.S.A.
Mailing Address:	16205 Roseleaf Lane Los Gatos, CA, 95032-3610

Full name of fourth Inventor:	Henry P. Moreton
Signature of fourth Inventor:	 Date: 9/30/04
Residence:	Woodside, CA
Citizenship:	U.S.A.
Mailing Address:	140 Phillip Road Woodside, CA, 94062-2625

Full name of fifth Inventor:	Earl A. Killian
Signature of fifth Inventor:	Date:
Residence:	Los Altos Hills, CA
Citizenship:	U.S.A.
Mailing Address:	27691 Central Drive Los Altos Hills, CA, 94022



Robert Greene Sterne
Edward J. Kessler
Jorge A. Goldstein
David K.S. Cornwell
Robert W. Esmond
Tracy-Gene G. Durkin
Michele A. Cimbala
Michael B. Ray
Robert E. Sokohl
Eric K. Steffe
Michael Q. Lee
Steven R. Ludwig
John M. Covert
Linda E. Alcom
Robert C. Millonig
Donald J. Featherstone
Lawrence B. Bugaisky
Michael V. Messinger

Judith U. Kim
Timothy J. Shea, Jr.
Patrick E. Garrett
Heidi L. Kraus
Edward W. Yee
Albert L. Ferro
Donald R. Banowitz
Peter A. Jackman
Teresa U. Medler
Jeffrey S. Weaver
Kendrick P. Patterson
Vincent L. Capuano
Eldora Ellison Floyd
Thomas C. Fiala
Brian J. Del Buono
Virgil Lee Beaton
Kimberly N. Reddick
Theodore A. Wood

Elizabeth J. Haanes
Joseph S. Ostroff
Frank R. Cottingham
Christine M. Lhulier
Rae Lynn Prensaman
Jane Shershenovich
George S. Bardmesser
Daniel A. Klein
Jason D. Eisenberg
Michael D. Specht
Andrea J. Kamage
Tracy L. Muller
LuAnne M. DeSantis
John J. Figueroa
Ann E. Summerfield
Tiera S. Coston
Aric W. Ledford
Jessica L. Parezo

Timothy A. Doyle*
Gaby L. Longworth*
Nicole D. Dretar*
Ted J. Ebersole
Jyoti C. Iyer*
Registered Patent Agents*
Karen R. Markowicz
Nancy J. Leith
Helene C. Carlson
Matthew J. Dowd
Aaron L. Schwartz
Katrina Y. Pei Quach
Bryan L. Skelton
Robert A. Schwartzman
Teresa A. Colella
Jeffrey S. Lundgren
Victoria S. Rutherford

Eric D. Hayes
Michelle K. Holoubek
Robert H. DeSelms
Simon J. Elliott
Julie A. Heider
Mita Mukherjee
Scott M. Woodhouse

Of Counsel
Kenneth C. Bass III
Evan R. Smith
Marvin C. Guthrie

*Admitted only in Maryland
*Admitted only in Virginia
*Practice Limited to
Federal Agencies

June 3, 2004

WRITER'S DIRECT NUMBER:
(202) 772-8629
INTERNET ADDRESS:
DONF@SKGF.COM

Timothy J. van Hook
224 Oakgrove Avenue
Atherton, CA 94027

Via Federal Express

Re: Declaration for U.S. Utility Patent Application
Application No. 09/662,832; Filed: September 15, 2000
For: **Alignment and Ordering of Vector Elements for Single Instruction
Multiple Data Processing**
Our Ref: 1778.0100002/DJF/LMY

Dear Mr. van Hook:

Further to your conversation with LuAnne DeSantis on June 2, 2004, enclosed please find a copy of the above-captioned patent application as filed in the United States Patent and Trademark Office (USPTO) on September 15, 2000, along with copies of four subsequently filed amendments for your review.

Also enclosed for your review and execution please find a "Supplemental Declaration for Patent Application." Once you have completed your review of the specification, drawings, and amendments, and if the information listed on the Declaration is correct and complete, we ask that you **sign** and **date** the Declaration in the space provided and return it to us using the enclosed self-addressed stamped envelope.

If, for any reason, you do not wish to execute the enclosed Declaration, we ask that you please review and execute the statement at the close of this letter. This statement simply verifies your receipt of this letter, states that you elected not to sign the enclosed Supplemental Declaration for the above-captioned currently pending patent application and states that you previously elected not to sign the Declaration for parent application 09/847,649. If the statement meets with your approval, please **sign** and **date** in the space provided below. Then, please return a copy of this letter to us in the enclosed self-addressed stamped envelope at your earliest possible convenience.

Timothy J. van Hook
June 3, 2004
Page 2

We greatly appreciate your assistance in this matter. If you have any questions, please do not hesitate to contact us.

Very truly yours,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



Donald J. Featherstone

DJF/LMY:krd
Enclosures

271715_1.DOC

I, Timothy J. van Hook, hereby state that I elect not to execute the Supplemental Declaration for Patent Application for currently pending U.S. Patent Application No. 09/662,832, filed September 15, 2000 (which is a continuation of U.S. Application No. 09/263,798, filed March 5, 1999, and U.S. Application No. 08/947,649, filed October 9, 1997) for the invention entitled **Alignment and Ordering of Vector Elements for Single Instruction Multiple Data Processing**, the specification and subsequent amendments to which have been provided to me for my review by Sterne, Kessler, Goldstein & Fox, P.L.L.C.

Furthermore, I hereby confirm my past election not to execute the Declaration for parent U.S. Application No. 08/947,649 in October 1997 and March 1998, the specification of which was provided to me by the Law Offices of Wagner, Murabito & Hao.

Signed: _____
Timothy J. van Hook

Date: _____

From: Origin ID: (202)371-2600
 Donald J. Featherstone
 Sterne Kessler Goldstein & Fox
 1100 New York Avenue, NW

Washington, DC 20005



Ship Date: 03JUN04
 Actual Wgt: 1 LB
 System#: 1162221/INET1800
 Account#: S *****

REF: 1778.0100002



Delivery Address Bar Code

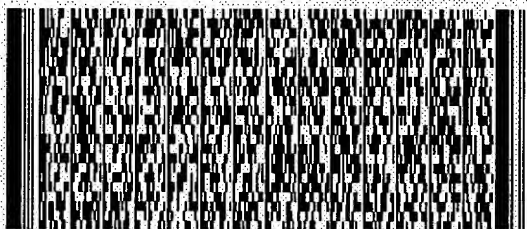
SHIP TO: (650)325-7605

BILL SENDER

Timothy J. van Hook

224 Oakgrove Avenue

Atherton, CA 94027



PRIORITY OVERNIGHT

FRI

Deliver By:
04JUN04

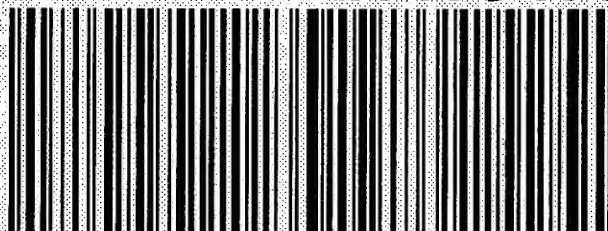
TRK# 7918 5741 6715

FORM
0201

SFO A2

94027 -CA-US

XH HGTA



Shipping Label: Your shipment is complete

1. Use the 'Print' feature from your browser to send this page to your laser or inkjet printer.
2. Fold the printed page along the horizontal line.
3. Place label in shipping pouch and affix it to your shipment so that the barcode portion of the label can be read and scanned.

Warning: Use only the printed original label for shipping. Using a photocopy of this label for shipping purposes is fraudulent and could result in additional billing charges, along with the cancellation of your FedEx account number.

Use of this system constitutes your agreement to the service conditions in the current FedEx Service Guide, available on fedex.com. FedEx will not be responsible for any claim in excess of \$100 per package, whether the result of loss, damage, delay, non-delivery, misdelivery, or misinformation, unless you declare a higher value, pay an additional charge, document your actual loss and file a timely claim. Limitations found in the current FedEx Service Guide apply. Your right to recover from FedEx for any loss, including intrinsic value of the package, loss of sales, income interest, profit, attorney's fees, costs, and other forms of damage whether direct, incidental, consequential, or special is limited to the greater of \$100 or the authorized declared value. Recovery cannot exceed actual documented loss. Maximum for items of extraordinary value is \$500, e.g. jewelry, precious metals, negotiable instruments and other items listed in our Service Guide. Written claims must be filed within strict time limits, see current FedEx Service Guide.

 **Sterne Kessler
Goldstein Fox**
ATTORNEYS AT LAW
1100 New York Avenue, NW
Washington, DC 20005



Sterne, Kessler, Goldstein & Fox P.L.L.C.
(Attention: LuAnne DeSantis)
1100 New York Avenue N.W.
Washington, D.C. 20005

Best Available Copy

Supplemental Declaration for Patent Application

Docket Number: 1778.0100002

As a below named inventor, I hereby declare that:

My residence, mailing address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter that is claimed and for which a patent is sought on the invention entitled **Alignment and Ordering of Vector Elements for Single Instruction Multiple Data Processing**, the specification of which is attached hereto unless the following box is checked:

- ☒ was filed on September 15, 2000, as United States Application Number 09/662,832 (which is a continuation of U.S. Application Number 09/263,798, filed March 5, 1999, which is a continuation of U.S. Application Number 08/947,649, filed October 9, 1997); and
was amended on September 15, 2000; April 9, 2001; January 24, 2002; and May 22, 2002.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or (f) or § 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or § 365(a) of any PCT international application, which designated at least one country other than the United States of America, listed below, and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Applications(s):

Priority Claimed

(Application No.)

(Country)

(Day/Month/Year Filed)

☐ Yes ☐ No

(Application No.)

(Country)

(Day/Month/Year Filed)

☐ Yes ☐ No

Send Correspondence to:

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 New York Avenue, N.W.
Washington, D.C. 20005-3934

Direct Telephone Calls to:

(202) 371-2600

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first Inventor:	Timothy J. van Hook
Signature of first Inventor:	Date:
Residence:	Atherton, CA
Citizenship:	U.S.A.
Mailing Address:	224 Oakgrove Avenue Atherton, CA 94027

Declaration for Patent Application

Docket Number: 1778.0100002

As a below named inventor, I hereby declare that:

My residence, mailing address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter that is claimed and for which a patent is sought on the invention entitled **Alignment and Ordering of Vector Elements for Single Instruction Multiple Data Processing**, the specification of which is attached hereto unless the following box is checked:

- ☒ was filed on September 15, 2000;
as United States Application Number 09/662,832; and
was amended on September 15, 2000; April 9, 2001; January 24, 2002; May 22, 2002; and June 18, 2004.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or (f) or § 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or § 365(a) of any PCT international application, which designated at least one country other than the United States of America, listed below, and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Applications(s):

Priority Claimed

(Application No.)

(Country)

(Day/Month/Year Filed)

☐ Yes ☐ No

(Application No.)

(Country)

(Day/Month/Year Filed)

☐ Yes ☐ No

Send Correspondence to:

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 New York Avenue, N.W.
Washington, D.C. 20005-3934

Direct Telephone Calls to:

(202) 371-2600

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first Inventor:	Timothy J. Van Hook
Signature of first Inventor:	Date:
Residence:	Atherton, CA
Citizenship:	U.S.A.
Mailing Address:	224 Oakgrove Avenue Atherton, CA, 94027

Full name of second Inventor:	Peter Yan-Tek Hsu
Signature of second Inventor:	Date:
Residence:	San Francisco, CA
Citizenship:	U.S.A.
Mailing Address:	1 Rausch Street, Unit F San Francisco, CA, 94103

Full name of third Inventor:	William A. Huffman
Signature of third Inventor:	Date:
Residence:	Los Gatos, CA
Citizenship:	U.S.A.
Mailing Address:	16205 Roseleaf Lane Los Gatos, CA, 95032-3610

Declaration for Patent Application

Docket Number: 1778.0100001

As a below named inventor, I hereby declare that:

My residence, mailing address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter that is claimed and for which a patent is sought on the invention entitled **Alignment and Ordering of Vector Elements for Single Instruction Multiple Data Processing**, the specification of which is attached hereto unless the following box is checked:

☒ was filed on March 5, 1999;
as United States Application Number 09/263,798 (now U.S. Patent No. 6,266,752 B1; Issued: July 24, 2001); and
was amended on September 1, 1999; May 1, 2000; and May 19, 2000.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or (f) or § 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or § 365(a) of any PCT international application, which designated at least one country other than the United States of America, listed below, and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Applications(s):

Priority Claimed

_____ (Application No.)	_____ (Country)	_____ (Day/Month/Year Filed)
_____ (Application No.)	_____ (Country)	_____ (Day/Month/Year Filed)

☐ Yes ☐ No

☐ Yes ☐ No

Send Correspondence to:

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 New York Avenue, N.W.
Washington, D.C. 20005-3934

Direct Telephone Calls to:

(202) 371-2600

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first Inventor:	Timothy J. Van Hook
Signature of first Inventor:	Date:
Residence:	Atherton, CA
Citizenship:	U.S.A.
Mailing Address:	224 Oakgrove Road Atherton, CA, 94027

Full name of second Inventor:	Peter Yan-Tek Hsu
Signature of second Inventor:	Date:
Residence:	San Francisco, CA
Citizenship:	U.S.A.
Mailing Address:	1 Rausch Street, Unit F San Francisco, CA, 94103

Full name of third Inventor:	William A. Huffman
Signature of third Inventor:	Date:
Residence:	Los Gatos, CA
Citizenship:	U.S.A.
Mailing Address:	16205 Roseleaf Lane Los Gatos, CA, 95032-3610

Full name of fourth Inventor:	Henry P. Moreton
Signature of fourth Inventor:	Date:
Residence:	Woodside, CA
Citizenship:	U.S.A.
Mailing Address:	140 Phillip Road Woodside, CA, 94062-2625

Full name of fifth Inventor:	Earl A. Killian
Signature of fifth Inventor:	Date:
Residence:	Los Altos Hills, CA
Citizenship:	U.S.A.
Mailing Address:	27961 Central Drive Los Altos Hills, CA, 94022

Declaration and Power of Attorney for a Patent Application

Declaration

As below named inventor, I hereby declare that my residence post office address, and citizenship are as stated below my name. Further, I hereby declare that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ALIGNMENT AND ORDERING OF VECTOR ELEMENTS FOR SINGLE INSTRUCTION MULTIPLE DATA PROCESSING

the specification of which:

..... is attached hereto, or
 X was filed on 10/9/97 as application serial no. 08/947,649 : and
 was amended on

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above; and

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

Foreign Priority Claim

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Number	Country	Date Filed	Priority Claimed
.....	yes no
.....	yes no

U.S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Serial Number	Filing Date	Status (patented/pending/abandoned)
.....
.....

Best Available Copy

Power of Attorney

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent Trademark Office connected therewith.

<u>James P. Hao</u>	Registration No.: <u>36,398</u>
<u>Anthony C. Murabito</u>	Registration No.: <u>35,295</u>
<u>John P. Wagner</u>	Registration No.: <u>35,398</u>
<u>Glenn D. Barnes</u>	Registration No.: <u>P-42,293</u>
<u>Wilfred H. Lam</u>	Registration No.: <u>P-41,923</u>
<u>Steve Weiner</u>	Registration No.: <u>38,330</u>
<u>Chris Byrne</u>	Registration No.: <u>32,204</u>
<u>Irene Fernandez</u>	Registration No.: <u>34,625</u>
<u>John Brigden</u>	Registration No.: <u>40,530</u>

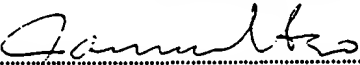
Send Correspondence to:

WAGNER, MURABITO & HAO
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Signatures

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor: Timothy J. van Hook

Inventor's Signature  Date 7/16/98
James P. Hao signing for Timothy J. van Hook under 37 C.F.R. § 1.47 (b)
 Residence Atherton, California Citizenship USA
 (City State)
 P.O. Address 224 Oakgrove Avenue, Atherton, California 94027

Full Name of Second/Joint Inventor: Peter Hsu

Inventor's Signature _____ Date _____
 Residence Fremont, California Citizenship _____
 (City State)
 P.O. Address 2853 Welk Common, Fremont, California 94555

Full Name of Third/Joint Inventor: William A. Huffman

Inventor's Signature _____ Date _____
 Residence Los Gatos, California Citizenship USA
 (City State)
 P.O. Address 16205 Roseleaf Lane, Los Gatos, California 95032

Full Name of Fourth/Joint Inventor: Henry P. Moreton

Inventor's Signature _____ Date _____
 Residence Woodside, California Citizenship USA
 (City State)
 P.O. Address 140 Phillip Road, Woodside, California 94062-2625

Full Name of Fifth/Joint Inventor: Earl A. Killian

Inventor's Signature _____ Date _____
 Residence Los Altos Hills, California Citizenship USA
 (City State)
 P.O. Address 27961 Central Drive, Los Altos Hills, California 94022

Declaration and Power of Attorney for a Patent Application

Declaration

As below named inventor, I hereby declare that my residence post office address, and citizenship are as stated below my name. Further, I hereby declare that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ALIGNMENT AND ORDERING OF VECTOR ELEMENTS FOR SINGLE INSTRUCTION MULTIPLE DATA PROCESSING

the specification of which:

..... is attached hereto, or
☒ was filed on 10/9/97 as application serial no. 08/947,649 : and
 was amended on

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above; and

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

Foreign Priority Claim

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Number	Country	Date Filed	Priority Claimed
.....	yes no
.....	yes no

U.S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Serial Number	Filing Date	Status (patented/pending/abandoned)
.....
.....

Best Available Copy

Power of Attorney

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent Trademark Office connected therewith.

James P. Hao	Registration No.: 36,398
Anthony C. Murabito	Registration No.: 35,295
John P. Wagner	Registration No.: 35,398
Glenn D. Barnes	Registration No.: P-42,293
Wilfred H. Lam	Registration No.: P-41,923
Steve Weiner	Registration No.: 38,330
Chris Byrne	Registration No.: 32,204
Irene Fernandez	Registration No.: 34,625
John Brigden	Registration No.: 40,530

Send Correspondence to:

WAGNER, MURABITO & HAO
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

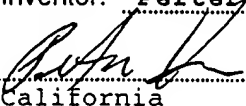
Signatures

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor: Timothy J. van Hook

Inventor's Signature _____ Date _____
Residence Atherton, California Citizenship USA
(City State)
P.O. Address 224 Oakgrove Avenue, Atherton, California 94027

Full Name of Second/Joint Inventor: Perter Hsu

Inventor's Signature  Date 3/4/98
Residence Fremont, California Citizenship _____
(City State)
P.O. Address 2853 Welk Common, Fremont, California 94555

Full Name of Third/Joint Inventor: William A. Huffman

Inventor's Signature _____ Date _____
Residence Los Gatos, California Citizenship USA
(City State)
P.O. Address 16205 Roseleaf Lane, Los Gatos, California 95032

Best Available Copy

Full Name of Fourth/Joint Inventor: Henry P. Moreton

Inventor's Signature

Date

Residence Woodside, California

Citizenship USA

(City State)

P.O. Address 140 Phillip Road, Woodside, California 94062-2625

Full Name of Fifth/Joint Inventor: Earl A. Killian

Inventor's Signature

Date

Residence Los Altos Hills, California

Citizenship USA

(City State)

P.O. Address 27961 Central Drive, Los Altos Hills, California 94022

Best Available Copy

Declaration and Power of Attorney for a Patent Application

Declaration

As below named inventor, I hereby declare that my residence post office address, and citizenship are as stated below my name. Further, I hereby declare that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ALIGNMENT AND ORDERING OF VECTOR ELEMENTS FOR SINGLE INSTRUCTION MULTIPLE DATA PROCESSING

the specification of which:

..... is attached hereto, or
☒ was filed on 10/9/97 as application serial no. 08/947,649 : and
 was amended on

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above; and

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

Foreign Priority Claim

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Number	Country	Date Filed	Priority Claimed
.....	yes no
.....	yes no

U.S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Serial Number	Filing Date	Status (patented/pending/abandoned)
.....
.....

Best Available Copy

Power of Attorney

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent Trademark Office connected therewith.

James P. Hao	Registration No.: 36,398
Anthony C. Murabito	Registration No.: 35,295
John P. Wagner	Registration No.: 35,398
Glenn D. Barnes	Registration No.: P-42,293
Wilfred H. Lam	Registration No.: P-41,923
Steve Weiner	Registration No.: 38,330
Chris Byrne	Registration No.: 32,204
Irene Fernandez	Registration No.: 34,625
John Brigden	Registration No.: 40,530

Send Correspondence to:

WAGNER, MURABITO & HAO
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Signatures

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor: Timothy J. van Hook

Inventor's Signature _____ Date _____
Residence Atherton, California Citizenship USA
(City State)
P.O. Address 224 Oakgrove Avenue, Atherton, California 94027

Full Name of Second/Joint Inventor: Perter Hsu

Inventor's Signature _____ Date _____
Residence Fremont, California Citizenship _____
(City State)
P.O. Address 2853 Welk Common, Fremont, California 94555

Full Name of Third/Joint Inventor: William A. Huffman

Inventor's Signature William A. Huffman Date May 5, 1998
Residence Los Gatos, California Citizenship USA
(City State)
P.O. Address 16205 Roseleaf Lane, Los Gatos, California 95032

Best Available Copy

Full Name of Fourth/Joint Inventor: Henry P. Moreton

Inventor's Signature _____ Date _____
Residence Woodside, California Citizenship USA
(City State)
P.O. Address 140 Phillip Road, Woodside, California 94062-2625

Full Name of Fifth/Joint Inventor: Earl A. Killian

Inventor's Signature _____ Date _____
Residence Los Altos Hills, California Citizenship USA
(City State)
P.O. Address 27961 Central Drive, Los Altos Hills, California 94022

Declaration and Power of Attorney for a Patent Application

Declaration

As below named inventor, I hereby declare that my residence post office address, and citizenship are as stated below my name. Further, I hereby declare that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ALIGNMENT AND ORDERING OF VECTOR ELEMENTS FOR SINGLE INSTRUCTION MULTIPLE DATA PROCESSING

the specification of which:

..... is attached hereto, or
☒ was filed on 10/9/97 as application serial no. 08/947,649 : and
 was amended on

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above; and

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

Foreign Priority Claim

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Number	Country	Date Filed	Priority Claimed
.....	yes no
.....	yes no

U.S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Serial Number	Filing Date	Status (patented/pending/abandoned)
.....
.....

Best Available Copy

Power of Attorney

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent Trademark Office connected therewith.

James P. Hao	Registration No.: 36,398
Anthony C. Murabito	Registration No.: 35,295
John P. Wagner	Registration No.: 35,398
Glenn D. Barnes	Registration No.: P-42,293
Wilfred H. Lam	Registration No.: P-41,923
Steve Weiner	Registration No.: 38,330
Chris Byrne	Registration No.: 32,204
Irene Fernandez	Registration No.: 34,625
John Brigden	Registration No.: 40,530

Send Correspondence to:

WAGNER, MURABITO & HAO
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Signatures

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor: Timothy J. van Hook

Inventor's Signature _____ Date _____
Residence Atherton, California Citizenship USA
(City State)
P.O. Address 224 Oakgrove Avenue, Atherton, California 94027


Full Name of Second/Joint Inventor: Perter Hsu

Inventor's Signature _____ Date _____
Residence Fremont, California Citizenship _____
(City State)
P.O. Address 2853 Welk Common, Fremont, California 94555

Full Name of Third/Joint Inventor: William A. Huffman

Inventor's Signature _____ Date _____
Residence Los Gatos, California Citizenship USA
(City State)
P.O. Address 16205 Roseleaf Lane, Los Gatos, California 95032

Best Available Copy

Full Name of Fourth/Joint Inventor: Henry P. MoretonInventor's Signature 

Date

2/6/98Residence Woodside, California
(City State)Citizenship USAP.O. Address 140 Phillip Road, Woodside, California 94062-2625Full Name of Fifth/Joint Inventor: Earl A. Killian

Inventor's Signature _____

Date _____

Residence Los Altos Hills, California
(City State)Citizenship USAP.O. Address 27961 Central Drive, Los Altos Hills, California 94022

Best Available Copy

Declaration and Power of Attorney for a Patent Application

Declaration

As below named inventor, I hereby declare that my residence post office address, and citizenship are as stated below my name. Further, I hereby declare that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ALIGNMENT AND ORDERING OF VECTOR ELEMENTS FOR SINGLE INSTRUCTION MULTIPLE DATA PROCESSING

the specification of which:

..... is attached hereto, or
☒ was filed on 10/9/97 as application serial no. 08/947,649 : and
 was amended on

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above; and

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

Foreign Priority Claim

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Number	Country	Date Filed	Priority Claimed
.....	yes no
.....	yes no

U.S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Serial Number	Filing Date	Status (patented/pending/abandoned)
.....
.....

Best Available Copy

Power of Attorney

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent Trademark Office connected therewith.

James P. Hao	Registration No.: 36,398
Anthony C. Murabito	Registration No.: 35,295
John P. Wagner	Registration No.: 35,398
Glenn D. Barnes	Registration No.: P-42,293
Wilfred H. Lam	Registration No.: P-41,923
Steve Weiner	Registration No.: 38,330
Chris Byrne	Registration No.: 32,204
Irene Fernandez	Registration No.: 34,625
John Brigden	Registration No.: 40,530

Send Correspondence to:

WAGNER, MURABITO & HAO
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Signatures

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor: Timothy J. van Hook

Inventor's Signature _____ Date _____
Residence Atherton, California Citizenship USA
(City State)
P.O. Address 224 Oakgrove Avenue, Atherton, California 94027

Full Name of Second/Joint Inventor: Peter Hsu

Inventor's Signature _____ Date _____
Residence Fremont, California Citizenship _____
(City State)
P.O. Address 2853 Welk Common, Fremont, California 94555

Full Name of Third/Joint Inventor: William A. Huffman

Inventor's Signature _____ Date _____
Residence Los Gatos, California Citizenship USA
(City State)
P.O. Address 16205 Roseleaf Lane, Los Gatos, California 95032

Best Available Copy

Full Name of Fourth/Joint Inventor: Henry P. Moreton

Inventor's Signature _____ Date _____
Residence Woodside, California Citizenship USA

(City State)
P.O. Address 140 Phillip Road, Woodside, California 94062-2625

Full Name of Fifth/Joint Inventor: Earl A. Killian

Inventor's Signature  Date 13 July 1998
Residence Los Altos Hills, California Citizenship USA

(City State)
P.O. Address 27961 Central Drive, Los Altos Hills, California 94022

Best Available Copy

Declaration for Patent Application

Docket Number: 1778.0100000

As a below named inventor, I hereby declare that:

My residence, mailing address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter that is claimed and for which a patent is sought on the invention entitled **Alignment and Ordering of Vector Elements for Single Instruction Multiple Data Processing**, the specification of which is attached hereto unless the following box is checked:

- ☒ was filed on October 9, 1997;
as United States Application Number 08/947,649 (now U.S. Patent No. 5,933,650; Issued: August 3, 1999); and
was amended on January 6, 1999, and February 1, 1999.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or (f) or § 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or § 365(a) of any PCT international application, which designated at least one country other than the United States of America, listed below, and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Applications(s):

Priority Claimed

(Application No.)

(Country)

(Day/Month/Year Filed)

☐ Yes ☐ No

(Application No.)

(Country)

(Day/Month/Year Filed)

☐ Yes ☐ No

Send Correspondence to:

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 New York Avenue, N.W.
Washington, D.C. 20005-3934

Direct Telephone Calls to:

(202) 371-2600

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first Inventor:	Timothy J. Van Hook
Signature of first Inventor:	Date:
Residence:	Atherton, CA
Citizenship:	U.S.A.
Mailing Address:	224 Oakgrove Road Atherton, CA, 94027

Full name of second Inventor:	Peter Yan-Tek Hsu
Signature of second Inventor:	Date:
Residence:	San Francisco, CA
Citizenship:	U.S.A.
Mailing Address:	1 Rausch Street, Unit F San Francisco, CA, 94103

Full name of third Inventor:	William A. Huffman
Signature of third Inventor:	Date:
Residence:	Los Gatos, CA
Citizenship:	U.S.A.
Mailing Address:	16205 Roseleaf Lane Los Gatos, CA, 95032-3610

Full name of fourth Inventor:	Henry P. Moreton
Signature of fourth Inventor:	Date:
Residence:	Woodside, CA
Citizenship:	U.S.A.
Mailing Address:	140 Phillip Road Woodside, CA, 94062-2625

Full name of fifth Inventor:	Earl A. Killian
Signature of fifth Inventor:	Date:
Residence:	Los Altos Hills, CA
Citizenship:	U.S.A.
Mailing Address:	27961 Central Drive Los Altos Hills, CA, 94022

Full name of fourth Inventor:	Henry P. Moreton
Signature of fourth Inventor:	Date:
Residence:	Woodside, CA
Citizenship:	U.S.A.
Mailing Address:	140 Phillip Road Woodside, CA, 94062-2625

Full name of fifth Inventor:	Earl A. Killian
Signature of fifth Inventor:	Date:
Residence:	Los Altos Hills, CA
Citizenship:	U.S.A.
Mailing Address:	27691 Central Drive Los Altos Hills, CA, 94022

**37 C.F.R. § 10.18(b) and (c): Effect of Signature and Certificate
for Correspondence Filed in the Patent and Trademark Office**

37 C.F.R. § 10.18(b): By presenting to the Office, (whether by signing, filing, submitting, or later advocating), any paper, the party presenting such paper, whether a practitioner or non-practitioner, is certifying that:

- (1) All statements made therein of the party's own knowledge are true, all statements made therein on information and belief are believed to be true, and all statements made therein are made with the knowledge that whoever, in any matter within the jurisdiction of the USPTO, knowingly and willfully falsifies, conceals, or covers up by any trick, scheme, or device a material fact, or makes any false, fictitious or fraudulent statements or representations, or makes or uses any false writing or document knowing the same to contain any false, fictitious or fraudulent statement or entry, shall be subject to the penalties set forth under 18 U.S.C. § 1001, and that violations of this paragraph may jeopardize the validity of the application or document, or the validity or enforceability of any patent, trademark registration, or certificate resulting therefrom; and
- (2) To the best of the party's knowledge, information and belief, formed after an inquiry reasonable under the circumstances, that:
 - (i) The paper is not being presented for any improper purpose, such as to harass someone or to cause unnecessary delay or needless increase in the cost of prosecution before the Office;
 - (ii) The claims and other legal contentions therein are warranted by existing law or by a nonfrivolous argument for the extension, modification, or reversal of existing law or the establishment of new law;
 - (iii) The allegations and other factual contentions have evidentiary support or, if specifically so identified, are likely to have evidentiary support after a reasonable opportunity for further investigation or discovery; and
 - (iv) The denials of factual contentions are warranted on the evidence, or if specifically so identified, are reasonably based on a lack of information or belief.

37 C.F.R. § 10.18(c): Violations of paragraph (b)(1), by a practitioner or a non-practitioner, may jeopardize the validity of the application or document, or the validity or enforceability of any patent, trademark registration, or certificate resulting therefrom. Violations of any of paragraphs (b)(2)(i) through (iv) of this section are, after notice and reasonable opportunity to respond, subject to such sanctions as deemed appropriate by the Commissioner, or the Commissioner's designee, which may include, but are not limited to, any combination of:

- (1) Holding certain facts to have been established;
- (2) Returning papers;
- (3) Precluding a party from filing a paper, or presenting or contesting an issue;
- (4) Imposing a monetary sanction;
- (5) Requiring a terminal disclaimer for the period of the delay; or
- (6) Terminating the proceedings in the Patent and Trademark Office.

Kristy Dahl - FedEx shipment 791344489555

From: FedEx <donotreply@fedex.com>
To: <donf@skgf.com>
Date: 9/23/2004 3:12 PM
Subject: FedEx shipment 791344489555

Our records indicate that the shipment sent from Donald J. Featherstone/Sterne Kessler Go to Henry P. Moreton has been delivered.

The package was delivered on 09/23/2004 at 10:49 AM and signed for or released by K.GREEN.

The ship date of the shipment was 09/22/2004.

The tracking number of this shipment was 791344489555.

FedEx appreciates your business. For more information about FedEx services, please visit our web site at <http://www.fedex.com>

To track the status of this shipment online please use the following:

[http://www.fedex.com/cgi-bin/tracking?
tracknumbers=791344489555&action=track&language=english&cntry_code=us](http://www.fedex.com/cgi-bin/tracking?tracknumbers=791344489555&action=track&language=english&cntry_code=us)

Disclaimer

FedEx has not validated the authenticity of any email address.

Kristy Dahl - FedEx shipment 791343579263

From: FedEx <donotreply@fedex.com>
To: <donf@skgf.com>
Date: 9/23/2004 4:10 PM
Subject: FedEx shipment 791343579263

Our records indicate that the shipment sent from Donald J. Featherstone/Sterne Kessler Go to Timothy J. Van Hook has been delivered.
The package was delivered on 09/23/2004 at 12:50 PM and signed for or released by .VANHOOK.

The ship date of the shipment was 09/22/2004.

The tracking number of this shipment was 791343579263.

FedEx appreciates your business. For more information about FedEx services, please visit our web site at <http://www.fedex.com>

To track the status of this shipment online please use the following:
http://www.fedex.com/cgi-bin/tracking?tracknumbers=791343579263&action=track&language=english&cntry_code=us

Disclaimer

FedEx has not validated the authenticity of any email address.

Kristy Dahl - FedEx shipment 792736103470

From: FedEx <donotreply@fedex.com>
To: <donf@skgf.com>
Date: 9/23/2004 10:41 PM
Subject: FedEx shipment 792736103470

Our records indicate that the shipment sent from Donald J. Featherstone/Sterne Kessler Go to William A. Huffman has been delivered.
The package was delivered on 09/23/2004 at 7:43 PM and signed for or released by W..HUFFMAN.

The ship date of the shipment was 09/22/2004.

The tracking number of this shipment was 792736103470.

FedEx appreciates your business. For more information about FedEx services, please visit our web site at <http://www.fedex.com>

To track the status of this shipment online please use the following:
[http://www.fedex.com/cgi-bin/tracking?
tracknumbers=792736103470&action=track&language=english&cntry_code=us](http://www.fedex.com/cgi-bin/tracking?tracknumbers=792736103470&action=track&language=english&cntry_code=us)

Disclaimer

FedEx has not validated the authenticity of any email address.

Kristy Dahl - FedEx shipment 791938175275

From: FedEx <donotreply@fedex.com>
To: <donf@skgf.com>
Date: 9/23/2004 3:02 PM
Subject: FedEx shipment 791938175275

Our records indicate that the shipment sent from Donald J. Featherstone/Sterne Kessler Go to Earl A. Killian has been delivered.

The package was delivered on 09/23/2004 at 11:09 AM and signed for or released by L.EE.

The ship date of the shipment was 09/22/2004.

The tracking number of this shipment was 791938175275.

FedEx appreciates your business. For more information about FedEx services, please visit our web site at <http://www.fedex.com>

To track the status of this shipment online please use the following:

[http://www.fedex.com/cgi-bin/tracking?
tracknumbers=791938175275&action=track&language=english&cntry_code=us](http://www.fedex.com/cgi-bin/tracking?tracknumbers=791938175275&action=track&language=english&cntry_code=us)

Disclaimer

FedEx has not validated the authenticity of any email address.

Kristy Dahl - FedEx shipment 792095057606

From: FedEx <donotreply@fedex.com>
To: <donf@skgf.com>
Date: 9/27/2004 1:54 PM
Subject: FedEx shipment 792095057606

Our records indicate that the shipment sent from Donald J. Featherstone/Sterne Kessler Go to Peter Yan-Tek Hsu has been delivered.

The package was delivered on 09/27/2004 at 10:47 AM and signed for or released by J.TRACY.

The ship date of the shipment was 09/22/2004.

The tracking number of this shipment was 792095057606.

FedEx appreciates your business. For more information about FedEx services, please visit our web site at <http://www.fedex.com>

To track the status of this shipment online please use the following:

[http://www.fedex.com/cgi-bin/tracking?
tracknumbers=792095057606&action=track&language=english&cntry_code=us](http://www.fedex.com/cgi-bin/tracking?tracknumbers=792095057606&action=track&language=english&cntry_code=us)

Disclaimer

FedEx has not validated the authenticity of any email address.

From: LuAnne DeSantis
To: peterhsu@cs.wisc.edu
Date: 11/30/04 4:22PM
Subject: Request for New Executed Declarations (1778.010)

Re: Request for New Executed Declarations
U.S. Pat. No. 5,933,650, Issued: August 3, 1999
U.S. Pat. No. 6,266,758, Issued: July 24, 2001
U.S. Pat. Appl. No. 09/662,832, Filed: September 15, 2000
**For: Alignment and Ordering of Vector Elements for
Single Instruction Multiple Data Processing**
Inventors: Van Hook *et al.*
SKGF Refs.: 1778.0100000, 1778.0100001, 1778.0100002

Dear Mr. Hsu:

We mailed a package to you (on September 22, 2004) requesting that you review the above-listed patents and application and that you sign and return new declarations for those patents and application. According to our records, the package was delivered to you on September 27, 2004 (signed for by "J.TRACY"). As explained in our letter accompanying the package, we are making this request, at the direction of the United States Patent and Trademark Office (USPTO), in order to correct an alleged filing error made by a previous law firm.

I unsuccessfully tried to reach you by email on October 20, 2004, and by telephone on October 29, 2004, to ask if you found time to review the package. Assuming you have now had time to review the package, I am contacting you to ask if you have any questions that may expedite your response to our request. If you do have any questions or would like to discuss the contents of the package, please feel free to call me at (202) 772-8657.

Please note that we need to file a response with the USPTO as soon as possible, and no later than December 14, 2004. If we do not receive a response from you by Monday, December 13, 2004, we will assume that you refuse to cooperate in prosecuting / maintaining the above-captioned patent application / patents. If you decide not to sign the declarations, we would appreciate a response that informs us of your refusal to sign.

Best regards,
LuAnne M. DeSantis

This electronic message transmission contains information from the law firm of Sterne, Kessler, Goldstein & Fox P.L.L.C. which may be confidential or privileged. The information is intended to be for the use of the individual or entity named above. If you are not the intended recipient, be aware that any disclosure, copying, distribution or use of the contents of this information is prohibited. If you have received this electronic transmission in error, please notify us by telephone or by electronic mail immediately and delete the message without copying or disclosing it.

LuAnne M. DeSantis, Associate
Sterne, Kessler, Goldstein & Fox P.L.L.C.
1100 New York Avenue N.W.
Washington, D.C. 20005

office: (202) 772-8657
main: (202) 371-2600
fax: (202) 371-2540
email: ldesanti@skgf.com

CC: Don Featherstone

From: LuAnne DeSantis
To: huffman@tensilica.com
Date: 10/20/04 4:28PM
Subject: Recent Request for New Executed Declarations (1778.010)

Re: Recent Request for New Executed Declarations
U.S. Pat. No. 5,933,650, Issued: August 3, 1999
U.S. Pat. No. 6,266,758, Issued: July 24, 2001
U.S. Pat. Appl. No. 09/662,832, Filed: September 15, 2000
For: **Alignment and Ordering of Vector Elements for
Single Instruction Multiple Data Processing**
Inventors: Van Hook *et al.*
SKGF Refs.: 1778.010000, 1778.0100001, 1778.0100002

Dear Mr. Huffman:

Further to my telephone conversation with you on September 9, 2004, we mailed a package to you (on September 22, 2004) requesting that you review the above-listed patents and application and that you sign and return new declarations for those patents and applications. As explained in our letter accompanying the package, we are making this request, at the direction of the United States Patent and Trademark Office, in order to correct an alleged filing error made by a previous law firm.

According to our records, the package was delivered to you on September 23, 2004. Assuming you have had time to review the package, I am contacting you to ask if you have any questions that may expedite your response to our request. If you do have any questions or would like to discuss the contents of the package, please feel free to call me at (202) 772-8657.

Best regards,
LuAnne M. DeSantis

This electronic message transmission contains information from the law firm of Sterne, Kessler, Goldstein & Fox P.L.L.C. which may be confidential or privileged. The information is intended to be for the use of the individual or entity named above. If you are not the intended recipient, be aware that any disclosure, copying, distribution or use of the contents of this information is prohibited. If you have received this electronic transmission in error, please notify us by telephone or by electronic mail immediately and delete the message without copying or disclosing it.

LuAnne M. DeSantis, Associate
Sterne, Kessler, Goldstein & Fox P.L.L.C.
1100 New York Avenue N.W.
Washington, D.C. 20005

office: (202) 772-8657
main: (202) 371-2600
fax: (202) 371-2540
email: ldesanti@skgf.com

CC: Don Featherstone

From: LuAnne DeSantis
To: huffman@tensilica.com
Date: 11/30/04 4:22PM
Subject: Request for New Executed Declarations (1778.010)

Re: Request for New Executed Declarations
U.S. Pat. No. 5,933,650, Issued: August 3, 1999
U.S. Pat. No. 6,266,758, Issued: July 24, 2001
U.S. Pat. Appl. No. 09/662,832, Filed: September 15, 2000
For: **Alignment and Ordering of Vector Elements for
Single Instruction Multiple Data Processing**
Inventors: Van Hook *et al.*
SKGF Refs.: 1778.0100000, 1778.0100001, 1778.0100002

Dear Mr. Huffman:

We mailed a package to you (on September 22, 2004) requesting that you review the above-listed patents and application and that you sign and return new declarations for those patents and application. As explained in our letter accompanying the package, we are making this request, at the direction of the United States Patent and Trademark Office (USPTO), in order to correct an alleged filing error made by a previous law firm.

I wanted to thank you for your voicemail message of October 30, 2004, in which you stated that you had not yet reviewed the package and therefore did not yet have any questions. Assuming you have now had time to review the package, I am contacting you to ask if you have any questions that may expedite your response to our request. If you do have any questions or would like to discuss the contents of the package, please feel free to call me at (202) 772-8657.

Please note that we need to file a response with the USPTO as soon as possible, and no later than December 14, 2004. If we do not receive a response from you by Monday, December 13, 2004, we will assume that you refuse to cooperate in prosecuting / maintaining the above-captioned patent application / patents. If you decide not to sign the declarations, we would appreciate a response that informs us of your refusal to sign.

Best regards,
LuAnne M. DeSantis

This electronic message transmission contains information from the law firm of Sterne, Kessler, Goldstein & Fox P.L.L.C. which may be confidential or privileged. The information is intended to be for the use of the individual or entity named above. If you are not the intended recipient, be aware that any disclosure, copying, distribution or use of the contents of this information is prohibited. If you have received this electronic transmission in error, please notify us by telephone or by electronic mail immediately and delete the message without copying or disclosing it.

LuAnne M. DeSantis, Associate
Sterne, Kessler, Goldstein & Fox P.L.L.C.
1100 New York Avenue N.W.
Washington, D.C. 20005

office: (202) 772-8657
main: (202) 371-2600
fax: (202) 371-2540
email: ldesanti@skgf.com

CC: Don Featherstone

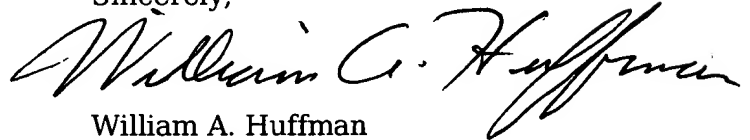
December 7, 2004

Donald J. Featherstone
Sterne, Kessler, Goldstein & Fox P.L.L.C.
1100 New York Avenue, NW
Washington, DC 20005-3934

Dear Mr. Featherstone,

I have received your request for new declaration documents for U.S. Patent No. 5,933,650, U.S. Patent No. 6,266,758, and U.S. Patent Application No. 09/622,832. I am familiar with Patent No. 5,933,650 from my original involvement with its filing and am glad to provide a new declaration to help with the apparently inadequate request for Rule 1.47 Status in the initial application. Unfortunately, I have never seen Patent No. 6,266, 758 or Patent Application No. 09/622,832 nor do I have the time to read them. I am, therefore, unable to assist you with the two additional declarations.

Sincerely,


William A. Huffman

RECEIVED

DEC 10 2004

Sterne, Kessler, Goldstein & Fox.
P.L.L.C.

SMJ SMJ 12/10/04
DJF Lvt 12/10

From: LuAnne DeSantis
To: earl@killian.com
Date: 10/25/04 8:09AM
Subject: Recent Request for New Executed Declarations (1778.010)

Re: Recent Request for New Executed Declarations
U.S. Pat. No. 5,933,650, Issued: August 3, 1999
U.S. Pat. No. 6,266,758, Issued: July 24, 2001
U.S. Pat. Appl. No. 09/662,832, Filed: September 15, 2000
**For: Alignment and Ordering of Vector Elements for
Single Instruction Multiple Data Processing**
Inventors: Van Hook *et al.*
SKGF Refs.: 1778.0100000, 1778.0100001, 1778.0100002

Dear Mr. Killian:

Further to my voicemail of September 1, 2004, we mailed a package to you (on September 22, 2004) requesting that you review the above-listed patents and application and that you sign and return new declarations for those patents and application. As explained in our letter accompanying the package, we are making this request, at the direction of the United States Patent and Trademark Office, in order to correct an alleged filing error made by a previous law firm.

According to our records, the package was delivered to you on September 23, 2004 (signed for by "L.EE"). Assuming you have had time to review the package, I am contacting you to ask if you have any questions that may expedite your response to our request. If you do have any questions or would like to discuss the contents of the package, please feel free to call me at (202) 772-8657.

Best regards,
LuAnne M. DeSantis

This electronic message transmission contains information from the law firm of Sterne, Kessler, Goldstein & Fox P.L.L.C. which may be confidential or privileged. The information is intended to be for the use of the individual or entity named above. If you are not the intended recipient, be aware that any disclosure, copying, distribution or use of the contents of this information is prohibited. If you have received this electronic transmission in error, please notify us by telephone or by electronic mail immediately and delete the message without copying or disclosing it.

LuAnne M. DeSantis, Associate
Sterne, Kessler, Goldstein & Fox P.L.L.C.
1100 New York Avenue N.W.
Washington, D.C. 20005

office: (202) 772-8657
main: (202) 371-2600
fax: (202) 371-2540
email: ldesanti@skgf.com

CC: Don Featherstone

From: LuAnne DeSantis
To: earl@killian.com
Date: 11/30/04 4:22PM
Subject: Request for New Executed Declarations (1778.010)

Re: Request for New Executed Declarations
U.S. Pat. No. 5,933,650, Issued: August 3, 1999
U.S. Pat. No. 6,266,758, Issued: July 24, 2001
U.S. Pat. Appl. No. 09/662,832, Filed: September 15, 2000
For: **Alignment and Ordering of Vector Elements for
Single Instruction Multiple Data Processing**
Inventors: Van Hook *et al.*
SKGF Refs.: 1778.0100000, 1778.0100001, 1778.0100002

Dear Mr. Killian:

We mailed a package to you (on September 22, 2004) requesting that you review the above-listed patents and application and that you sign and return new declarations for those patents and application. As explained in our letter accompanying the package, we are making this request, at the direction of the United States Patent and Trademark Office (USPTO), in order to correct an alleged filing error made by a previous law firm.

In a telephone conversation with you on October 29, 2004, you stated that you would consider reviewing the package and call if you had any questions. Assuming you found time to review the package, I am contacting you to ask if you have any questions that may expedite your response to our request. If you do have any questions or would like to discuss the contents of the package, please feel free to call me at (202) 772-8657.

Please note that we need to file a response with the USPTO as soon as possible, and no later than December 14, 2004. If we do not receive a response from you by Monday, December 13, 2004, we will assume that you refuse to cooperate in prosecuting / maintaining the above-captioned patent application / patents. If you decide not to sign the declarations, we would appreciate a response that informs us of your refusal to sign.

Best regards,
LuAnne M. DeSantis

This electronic message transmission contains information from the law firm of Sterne, Kessler, Goldstein & Fox P.L.L.C. which may be confidential or privileged. The information is intended to be for the use of the individual or entity named above. If you are not the intended recipient, be aware that any disclosure, copying, distribution or use of the contents of this information is prohibited. If you have received this electronic transmission in error, please notify us by telephone or by electronic mail immediately and delete the message without copying or disclosing it.

LuAnne M. DeSantis, Associate
Sterne, Kessler, Goldstein & Fox P.L.L.C.
1100 New York Avenue N.W.
Washington, D.C. 20005

office: (202) 772-8657
main: (202) 371-2600
fax: (202) 371-2540
email: ldesanti@skgf.com

CC: Don Featherstone

LuAnne DeSantis - Re: Request for New Executed Declarations (1778.010)

From: "Earl A. Killian" <earl@killian.com>
To: "LuAnne DeSantis" <LDESANTI@skgf.com>
Date: 12/1/2004 11:59 AM
Subject: Re: Request for New Executed Declarations (1778.010)
CC: "Don Featherstone" <DONF@skgf.com>

I have not yet had a chance to review the revised declaration, and since I do not feel it is possible to sign it without a thorough review, I suggest you go ahead and execute the application without my signature, as you indicated you would do for some of the other applicants on the phone.

I apologize that I cannot be more helpful, but the reading patents is particularly tedious work, and I don't feel like this is a good use of my time just now.

-Earl

UNITED STATES PATENT APPLICATION
FOR

ALIGNMENT AND ORDERING OF VECTOR ELEMENTS FOR SINGLE
INSTRUCTION MULTIPLE DATA PROCESSING

Inventors:

Timothy J. van Hook

Peter Hsu

William Huffman

Henry P. Moreton

Earl Killian

Prepared by:

WAGNER, MURABITO & HAO

Two North Market Street

Third Floor

San Jose, California 95113

ALIGNMENT AND ORDERING OF VECTOR ELEMENTS FOR SINGLE INSTRUCTION MULTIPLE DATA PROCESSING

FIELD OF THE INVENTION

5 The present invention relates to the field of single instruction multiple data vector (SIMD) processing. More particularly, the present claimed invention relates to alignment and ordering vector elements for SIMD processing.

10 BACKGROUND ART

Today, most processors in microcomputer systems provide a 64-bit wide datapath architecture. The 64-bit datapath allows operations such as read, write, add, subtract, and multiply on the entire 64 bits of data at once. However, for many applications the types of data involved simply do not
15 require the full 64 bits. In media signal processing (MDMX) applications, for example, the light and sound values are usually represented in 8, 12, 16, or 24 bit numbers. This is because people typically are not able to distinguish the levels of light and sound beyond the levels represented by these numbers of bits. Hence, data types in MDMX applications typically require less than the
20 full 64 bits provided in the datapath in most computer systems.

To efficiently utilize the entire datapath, the current generation of processors typically utilizes a single instruction multiple data (SIMD) method. According to this method, a multitude of smaller numbers are packed into
25 the 64 bit doubleword as elements, each of which is then operated on independently and in parallel. Prior Art Figure 1 illustrates an exemplary single instruction multiple data (SIMD) method. Registers, vs and vt, in a

processor are of 64-bit width. Each register is packed with four 16-bit data elements fetched from memory: register vs contains vs[0], vs[1], vs[2], and vs[3] and register vt contains vt[0], vt[1], vt[2], and vt[3]. The registers in essence contain a vector of N elements. To add elements of matching index, an add instruction adds, independently, each of the element pairs of matching index from vs and vt. A third register, vd, of 64-bit width may be used to store the result. For example, vs[0] is added to vt[0] and its result is stored into vd[0]. Similarly, vd[1], vd[2], and vd[3] store the sum of vs and vt elements of corresponding indexes. Hence, a single add operation on the 64-bit vector results in 4 simultaneous additions on each of the 16-bit elements. On the other hand, if 8-bit elements were packed into the registers, one add operation performs 8 independent additions in parallel. Consequently, when a SIMD arithmetic instruction such as addition, subtraction, or multiply, is performed on the data in the 64-bit datapath, the operation actually performs multiple numbers of operations independently and in parallel on each of the smaller elements comprising the 64 bit datapath. In SIMD vector operation, processors typically require alignment to the data type size of 64-bit doubleword on a load. This alignment ensures that the SIMD vector operations occur on aligned boundaries of a 64-bit doubleword boundary.

Unfortunately, the elements within application data vectors are frequently not 64-bit doubleword aligned for SIMD operations. For example, data elements stored in a memory unit are loaded into registers in a chunk such as a 64-bit doubleword format. To operate on the individual elements, the elements are loaded into a register. The order of the elements in the register remain the same as the order in the original memory. Accordingly, the elements may not be properly aligned for a SIMD operation.

Traditionally, when elements are not aligned with a proper boundary as required for a SIMD vector operation, the non-aligned vector processing have typically been reduced to scalar processing. That is, operations took
5 place one element at a time instead of simultaneous multiple operations. Consequently, SIMD vector operations lost parallelism and performance advantages when the vector elements were not properly aligned.

Furthermore, many media applications require a specific ordering for
10 the elements within a SIMD vector. Since elements necessary for SIMD processing are commonly stored in multiple 64-bit doublewords with other elements, these elements need to be selected and assembled into a vector of desired order. For example, multiple channel data are commonly stored in separate arrays or interleaved in a single array. Processing the data requires
15 interleaving or deinterleaving the multiple channels. Other applications require SIMD vector operations on transposed 2 dimensional arrays of data. Yet other applications reverse the order of elements in an array as in FFTs, DCTs, and convolution algorithms.

20 Thus, what is needed is a method for aligning and ordering elements for more efficient SIMD vector operations by providing computational parallelism.

SUMMARY OF THE INVENTION

The present invention provides alignment and ordering of vector elements for SIMD processing. The present invention is implemented in a computer system including a processor having a plurality of registers. In the
5 alignment of vector elements for SIMD processing, one vector is loaded from a memory unit into a first register and another vector is loaded from the memory unit into a second register. The first vector contains a first byte of an aligned vector to be generated. Then, a starting byte specifying the first byte of an aligned vector is determined. Next, a vector is extracted from the first
10 register and the second register beginning from the first bit in the first byte of the first register continuing through the bits in the second register. Finally, the extracted vector is replicated into a third register such that the third register contains a plurality of elements aligned for SIMD processing. In the ordering of vector elements for SIMD processing, a first vector is loaded from
15 a memory unit into a first register and a second vector is loaded from the memory unit into a second register. Then, a subset of elements is selected from the first register and the second register. The elements from the subset are then replicated into the elements in the third register in a particular order suitable for subsequent SIMD vector processing.

20

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention:

5

Prior Art Figure 1 illustrates an exemplary single instruction multiple data (SIMD) instruction method.

Figure 2 illustrates a block diagram of an exemplary computer system for implementing the present invention.

10 Figure 3 illustrates a block diagram of an exemplary datapath for aligning and ordering vector elements.

Figure 4 illustrates a block diagram of an alignment unit in a processor for aligning a vector of elements.

15 Figure 5 illustrates a flow diagram of the steps involved in extracting an aligned vector from two exemplary vectors.

Figure 6A illustrates a block diagram of a full byte-mode crossbar circuit used in generating a vector of elements from elements of two vector registers.

Figure 6B shows a more detailed diagram of the operation of an exemplary AND gate associated with element 7 in the first register, vs.

20 Figure 7 illustrates shuffle operations for ordering 8-bit elements in a 64-bit doubleword.

Figure 8A illustrates a block diagram of a shuffle operation, which converts four unsigned upper bytes (i.e., 8 bits) in a source register to four 16-bit halves in a destination register.

25 Figure 8B illustrates a block diagram of a shuffle operation, which converts a vector of unsigned low 4 bytes from a source register to four 16-bit halves in a destination register.

Figure 8C illustrates a block diagram of a shuffle operation, which converts a vector of signed upper 4 bytes from a source register to four 16-bit halves in a destination register by replicating the signs across the upper bytes in the halves.

5 Figure 8D illustrates a block diagram of a shuffle operation, which converts a vector of signed low 4 bytes from a source register to four 16-bit halves in a destination register by replicating the signs across the upper bytes in the halves.

10 Figure 8E illustrates a block diagram of a shuffle operation, which replicates the odd elements of 8 8-bit elements from each of two source registers into 8 elements in a destination vector register.

Figure 8F illustrates a block diagram of a shuffle operation, which replicates the even elements of 8 8-bit elements from each of two source registers into 8 elements in a destination vector register.

15 Figure 8G illustrates a block diagram of a shuffle operation, which replicates the upper 4 elements of 8 8-bit elements from each of two source registers into 8 elements in a destination vector register.

20 Figure 8H illustrates a block diagram of a shuffle operation, which replicates the lower 4 elements of 8 8-bit elements from each of two source registers into 8 elements in a destination vector register.

Figure 9 illustrates shuffle operations for ordering 16-bit elements in a 64-bit doubleword.

25 Figure 10A illustrates a block diagram of a shuffle operation, which replicates the upper 2 elements of 4 16-bit elements from each of two source registers into 4 elements in a destination vector register.

Figure 10B illustrates a block diagram of a shuffle operation, which replicates the lower 2 elements of 4 16-bit elements from each of two source registers into 4 elements in a destination vector register.

5 Figure 10C illustrates a block diagram of a shuffle operation, which replicates 2 odd elements of 4 16-bit elements from each of two source registers into 4 elements in a destination vector register.

Figure 10D illustrates a block diagram of a shuffle operation, which replicates 2 even elements of 4 16-bit elements from each of two source registers into 4 elements in a destination vector register.

10 Figure 10E illustrates a block diagram of a shuffle operation, which replicates even elements 0 and 2 from one source register into odd elements 1 and 3 in a destination vector register and further replicates odd elements 1 and 3 from another source register into the even elements 0 and 2, respectively, of the destination vector register.

15 Figure 10F illustrates a block diagram of a shuffle operation, which replicates even elements 0 and 2 from one source register into odd elements 3 and 1, respectively, in a destination vector register and further replicates odd elements 1 and 3 from another source register into the even elements 2 and 0, respectively, of the destination vector register.

20 Figure 10G illustrates a block diagram of a shuffle operation, which replicates the upper 2 elements of 4 16-bit elements from each of two source registers into a destination vector register.

Figure 10H illustrates a block diagram of a shuffle operation, which replicates the lower 2 elements of 4 16-bit elements from each of two source registers into a destination vector register.

25

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one skilled in the art that the present invention may be practiced without these specific details. In other instances well known methods, procedures, components, and circuits have not been described in detail so as not to unnecessarily obscure aspects of the present invention.

The present invention, a method for providing alignment and ordering of vector elements for single-instruction multiple-data (SIMD) processing, is described. The preferred embodiment of the present invention provides elements aligned and ordered for an efficient SIMD vector operation in a processor having 64-bit wide datapath within an exemplary computer system described below. Although such a datapath is exemplified herein, the present invention can be readily adapted to suit other datapaths of varying widths.

COMPUTER SYSTEM ENVIRONMENT

Figure 2 illustrates an exemplary computer system 200 comprised of a system bus 206 for communicating information, a processor 202 coupled with the bus 206 for processing information and instructions, a computer readable volatile memory unit 210 (e.g., random access memory, static RAM, dynamic RAM, etc.) coupled with the bus 206 for storing information and instructions for the processor 202, a computer readable non-volatile memory unit 208 (e.g., read only memory, programmable ROM, flash memory, EPROM, EEPROM, etc.) coupled with the bus 206 for storing static information and instructions

for the processor 202. A vector register file 204 containing a plurality of registers is included in the processor 202. In the present invention, the term vector register file 204 encompasses any register file containing a plurality of registers and as such is not limited to vector register files.

5

The computer system 200 of Figure 2 further includes a mass storage computer readable data storage device 212 (hard drive, floppy, CD-ROM, optical drive, etc.) such as a magnetic or optical disk and disk drive coupled with the bus 206 for storing information and instructions. Optionally, the computer system 200 may include a display device 214 coupled to the bus 206 for displaying information to the user, an alphanumeric input device 216 including alphanumeric and function keys coupled to the bus 206 for communicating information and command selections to the processor 202, a cursor control device 218 coupled to the bus 206 for communicating user input information and command selections to the processor 202, and a signal generating device 220 coupled to the bus 206 for communicating command selections to the processor 202.

According to an exemplary embodiment of the present invention, the processor 202 includes a SIMD vector unit that functions as a coprocessor for or as an extension of the processor 202. The SIMD vector unit performs various arithmetic and logical operations on each data element within a SIMD vector in parallel. The SIMD vector unit utilizes the register files of the processor 202 to hold SIMD vectors. The present invention may include one or more SIMD vector units to perform specialized operations such as arithmetic operations, logical operations, etc.

Figure 3 illustrates a block diagram of an exemplary datapath 300 for aligning and ordering vector elements. The datapath 300 includes a SIMD vector unit 302, an alignment unit 322, a register file 304, a crossbar circuit 314, and a vector load/store unit 302. The vector load/store unit 302 performs load and store functions. It loads a vector from memory into one of the registers in the register file 304. It also stores a vector from one of the registers in the register file 304 into main memory. The alignment unit 312 receives two vectors from two source registers such as vs 306 and vt 308. Then, the alignment unit 312 extracts an aligned vector from the two vectors and stores it into a destination register such as vd 310. The crossbar circuit 314 also receives two vectors two exemplary source registers, vs 306 and vt 308. The crossbar circuit 314 then selects a set of elements from the source registers and routes each of the elements in the selected set to a specified element in the exemplary destination register, vd 310. In an alternative embodiment, the crossbar circuit 314 may receive one vector from a single source register and select a set of elements from the vector. The data path 318 allows a result to be forwarded to the register file 304 or to the vector load/store unit to be stored into main memory.

The SIMD vector unit 302 represents a generic SIMD vector processing unit, which may be an arithmetic unit, logical unit, integer unit, etc. The SIMD vector unit 302 may receive either one or two vectors from one or two source registers. It should be appreciated that the present invention may include more than one SIMD vector unit performing various functions. The SIMD vector unit 302 may execute an operation specified in the instruction on each element within a vector in parallel.

The exemplary vector register file 304 is preferably comprised of 32 64-bit general purpose registers. To this end, the preferred embodiment of the present invention utilizes the floating point registers (FGR) of a floating point unit (FPU) in the processor as its vector registers. In this shared arrangement, data is moved between the vector register file 304 and a memory unit through the vector load/store unit 302. These load and store operations are unformatted. That is, no format conversions are performed and therefore no floating-point exceptions can occur due to these operations. Similarly, data is moved between the vector register file 304 and the alignment unit 312, the crossbar circuit 314, or the SIMD vector unit 316 without format conversions, and thus no floating-point exception occurs.

The present invention allows data types of 8-, 16-bit, 32-, or 64-bit fields. Hence, a 64-bit doubleword vector may contain 8 8-bit elements, 4 16-bit elements, 2 32-bit elements, or 1 64-bit element. According to this convention, vector registers of the present invention are interpreted in the following data formats: Quad Half (QH), Oct Byte (OB), Bi word (BW), and Long (L). In QH format, a vector register is interpreted as having 16-bit elements. For example, a 64-bit vector register is interpreted as a vector of 4 signed 16-bit integers. OB format interprets a vector register as being comprised of 8-bit elements. Hence, an exemplary 64-bit vector register is seen as a vector of 8 unsigned 8-bit integers. In BW format, a vector register is interpreted as having 2 32-bit elements. L format interprets a vector register as having a 64-bit element. These data types are provided to be adaptable to various register sizes of a processor. As described above, data format conversion is not necessary between these formats and floating-point format.

According to a preferred embodiment of the present invention, exemplary source registers, vs and vt, are each used to hold a set of vector elements. A third exemplary vector register, vd, is created from the source registers and holds a set of elements selected from the source registers.

- 5 Although the registers, vs, vt, and vd, are used to associate vector registers with a set of vector elements, other vector registers are equally suitable for present invention.

LOAD/STORE INSTRUCTIONS

- 10 The load and store instructions of the present invention use a special load/store unit to load and store a 64-bit doubleword between a register in a register file such as an FPR and a memory unit. The doubleword is loaded through an exemplary load/store unit 302 illustrated above in Figure 3. The load/store unit performs loading or storing of a doubleword with upper 61
15 bits of an effective address. The lowest 3 bits specify a byte address within the 64-bit doubleword for alignment.

- According to a preferred embodiment, an effective address is formed by adding the contents of an index value in a general purpose register (GPR) to a
20 base address in another GPR. The effective address is doubleword aligned. During the loading process, the last three bits of the effective address are ignored by treating these bits as 0s. Hence, the effective address is comprised of bits 3 to 63. The three bits from 0 to 2 contain the byte address for accessing individual bytes within a doubleword and are ignored by treating the three
25 bits as 0s. If the size of a register in a register file is 64-bits, then the 64-bit data stored in memory at the effective address is fetched and loaded into the register. If on the other hand, the size of the register in the register file is 32-

bits, then the lower 32 bits of the data are loaded into the vector register and the upper 32 bits of the data are loaded into the next register in sequence. Hence, a pair of 32-bit registers are used to hold a 64-bit data from the memory.

5

Conversely, the store instruction stores a doubleword from a vector register such as an FPR to the memory while ignoring alignment. The store operation is carried out through the exemplary load/store unit 302 illustrated above in Figure 3. The contents of a 64-bit doubleword in FPR, fs, is stored at the memory location specified by the effective address. The contents of GPR index and GPR base are added to form the effective address. The effective address is doubleword aligned. The last three bits of the effective address are ignored.

10

15

The effective address is formed by adding the contents of an index value in a general purpose register (GPR) to a base address in another GPR while ignoring the lowest three bits of the effective address by interpreting them as 0s. That is, the effective address is comprised of bits 3 to 63. The ignored three bits contain the byte address for accessing individual bytes within a doubleword. If the size of a vector register is 64-bits, then the content of the vector register is stored into memory. If on the other hand, the size of a vector register is 32-bits, then the lower 32 bits of the data are concatenated with the upper 32 bits of the data contained in the next register in sequence. Then, the concatenated 64-bit doubleword is stored into memory at the address specified by the effective address.

20

25

ALIGNMENT INSTRUCTION

The present alignment instruction operates on two 64-bit doublewords loaded into two registers from memory by issuing two load instructions. One doubleword is loaded into a first register (vs) and the other doubleword is
5 loaded into a second register (vt). The alignment instruction generates a 64-bit doubleword vector in a third register (vd) aligned for a SIMD vector operation. Preferably, an alignment unit performs alignment of a vector by funnel shift to extract an aligned 64-bit vector of elements from the two 64-bit registers.

10

Figure 4 illustrates a block diagram of an alignment unit in a processor for aligning a vector of elements. The vector load/store unit 404 loads two vectors from main memory 402 into two vector registers, vs and vt, in a register file 408. The alignment unit 410 receives the two vectors in the
15 vector registers, vs and vt, and extracts a byte aligned vector. Three control lines 412 representing three bits for the byte address controls the byte alignment performed through the alignment unit 410. The aligned vector is then forwarded to an exemplary vector register, vd, in the register file.

20

The alignment of a vector is dependent on a byte ordering mode of a processor. Byte ordering within a larger data size such as a 64-bit doubleword may be configured in either big-endian or little-endian order. Endian order refers to the location of byte 0 within a multi-byte data. A processor according to the present invention may be configured as either a big-endian or little-
25 endian system. For example, in a little-endian system, byte 0 is the least significant (i.e., rightmost) byte. On the other hand, in a big-endian system, byte 0 is the most significant (i.e., leftmost) byte. In the present invention, an

exemplary processor uses byte addressing for a doubleword access, which is aligned on a byte boundary divisible by eight (i.e., 0, 8, 16, ..., 56). Hence, a 64-bit doubleword loaded into a register in a processor is byte-aligned in either a big-endian or a little-endian mode. For a little-endian mode processor, the starting (i.e., first) byte for a vector to be extracted lies in the second vector register. Conversely for a big-endian mode processor, the starting (i.e., first) byte for the vector resides in the first vector register.

Figure 5 illustrates a flow diagram of the steps involved in extracting an aligned vector from two exemplary vectors. In step 502, two 64-bit doublewords are loaded from a memory unit into two 64-bit registers. One 64-bit doubleword is loaded into a first register and the other 64-bit doubleword in memory is loaded into the second register. Preferably, the former doubleword and the next doubleword are stored in contiguous memory space and their starting addresses differ by 64-bits or 8 bytes. The loading of the doublewords are accomplished through a load/store unit according to the load instruction described above.

The starting byte address of the aligned vector to be extracted is then determined in step 704. According to the preferred embodiment, the register and vector are all 64-bit wide. Since a 64-bit doubleword contains 8 bytes, three bits are needed to specify all the byte positions in a 64-bit doubleword. Hence, the preferred embodiment uses 3 bits to specify the position of the starting byte address in a 64-bit vector.

In one embodiment of the present invention, an alignment instruction provides an immediate, which is a constant byte address within a

doubleword. Preferably, the immediate consists of 3 bits for specifying a constant byte address to a byte among 8 bytes each in the first register (i.e., little-endian mode processor) and the second register (i.e., bit-endian mode processor). This alignment instruction performs a constant alignment of a
5 vector. The align amount is computed by masking the immediate, then using that value to control a funnel shift of vector vs concatenated with vector vt. The operands can be in the QH, OB, or BW format.

In an alternative embodiment, the alignment instruction provides a
10 variable byte addressing by specifying an address of a general purpose register (GPR) containing the starting byte address in the first register. This instruction accesses the GPR by using the address provided in the alignment instruction. Then, the instruction extracts the lower 3 bits in the GPR to obtain the starting byte address in the first register (i.e., little-endian mode) or
15 the second register (i.e., big-endian mode). The align amount is computed by masking the contents of GPR, rs, then using that value to control a funnel shift of vector vs concatenated with vector vt. The operands can be in QH, OB, or BW format.

20 After determining the starting byte address in step 504 of the flowchart in Figure 5, the first bit of the starting byte address is determined in step 506 by multiplying the starting byte address by 8. For example, if the starting byte address were 3, the first bit of the starting byte address is 3×8 or 24. Then in step 508, a 64-bit doubleword is extracted by concatenating from the first bit at
25 the starting byte address in one register continuing through the other register. This concatenation is accomplished by funnel shifting from the first bit of the starting byte. Specifically, the first register is assigned bit positions from 0 to

63. The second register is assigned the next 64 bit positions from 64 to 127. The extraction scheme depends on the byte ordering modes. A variable s , representing the first bit position at the starting byte address, can be used to simplify the illustration of the differences between the byte ordering modes.

- 5 In a big-endian byte mode, the concatenation occurs from bit position $127-s$ to $64-s$. Conversely, in a little-endian byte mode, the concatenation occurs from bit position s through $63+s$.

Then in step 510, the extracted vector is replicated into a destination register in the register file for SIMD vector processing. In an alternative, embodiment, the extracted vector may be stored into the memory unit for later use. The process then terminates in step 512.

SHUFFLE INSTRUCTION

- 15 The shuffle instruction according to the present invention provides a vector of ordered elements selected from either one or two other vector registers. One or more load/store instructions are used to load the vector(s) into registers for shuffle operation. One embodiment uses a full byte-mode crossbar to generate a vector of elements selected from the elements of two other exemplary vectors. That is, selected elements of the exemplary vectors, vs and vt , are merged into a new exemplary vector, vd . The new vector, vd , contains elements aligned for SIMD operation. Alternatively, a plurality of shuffle operations may be carried out to arrange the elements in a desired order for SIMD vector processing.

25

Figure 6A illustrates a block diagram of a full byte-mode crossbar circuit 600 used in generating a vector of elements from elements of two registers.

First, two vectors from a memory unit are loaded into two exemplary registers in a processor; the elements of the first vector are loaded into the first register, vs 602, and the elements of the second vector are loaded into the second register, vt 604. The elements of these two vector registers, vs 602 and vt 604, serve as source elements. The crossbar circuit 600 receives as input each of the elements from the two vector registers in parallel. A set of control lines 608 is coupled to the crossbar circuit 600 to relay a specific shuffle instruction operation. The shuffle instruction operation encodes a destination element for each of the selected source elements. In response to the specific shuffle instruction operation signals, the crossbar circuit 600 selects a set of elements from the two registers, vs 602 and vt 604, and routes or replicates each element to its associated destination element in an exemplary destination register, vd 606.

In addition, the present invention allows zeroing and sign extension of elements. For example with reference to Figure 6A, the present invention provides either zeroing or sign extension for each element in the first register, vs 602. In addition to providing the entire bits to the crossbar circuit 600, elements 0 through 7 in the first register, vs 602, provides their corresponding sign bits 612, 614, 616, 618, 620, 622, 624, and 626 (612 through 626) to the associated AND gates 628, 630, 632, 634, 636, 638, 640, and 642 (628 through 642). Each of the AND gates 628 through 642 also receives as the other input, a control signal 610, which originate from a specific shuffle instruction for specifying either zeroing or sign extension mode.

Figure 6B shows a more detailed diagram of the operation of the exemplary AND gate 628 associated with element 7 in the first register, vs 602.

The AND gate 628 receives a single sign bit 612 from the most significant bit in the element 7 of the first register, vs 602. The AND gate 628 also receives the control signal 610. To provide zeroing for element 7 for example, the control signal 610 inputs a 0 into the AND gate 628. In this case, the output
5 652 at the AND gate 628 is 0 no matter what the input is at the sign bit 612. On the other hand, when the control signal is 1, the AND gate 628 generates the sign bit 612 as the output 652, whatever the sign is. In both cases of zeroing and sign extension, the output 652 is routed to a plurality of output lines 654 for replicating the output signal into an appropriate width. Preferably, the
10 output lines 654 matches the number of bits in each element in the first register, vs 602. The crossbar circuit 600 accepts the signals on these output lines 652 and uses these signals to zero or sign extend element 7 when necessary according to a shuffle instruction. The AND gates for the other elements 0 to 6 operate in a similar manner to provide zeroing and sign
15 extension bit signals to the crossbar circuit 600.

The preferred embodiment of the present invention operates on vectors of elements in a preferred OB or QH mode. In an OB mode, a 64-bit doubleword vector is interpreted as having 8 8-bit elements. In a QH mode,
20 the 64-bit vector is treated as containing 4 16-bit elements. For example, in OB mode, the crossbar circuit 600 selects, in parallel, as source elements eight 8-bit elements among the elements in the registers vs 602 and vt 604. Each of the eight elements is then replicated or routed into a particular destination element in the destination vector register, vd 606. In QH mode, the crossbar
25 circuit selects four 16-bit elements and replicates or routes each element into a particular destination element in the destination register. Those skilled in the art will appreciate that the crossbar circuit represents one embodiment of

the present invention in implementing the shuffle instruction operations. A crossbar circuit is well known the art and is commonly used in conjunction with vector processing units.

5 Figure 7 illustrates shuffle operations for ordering 8-bit elements in a 64-bit doubleword. Each row represents the destination vector register, vd, comprised of 8 elements, vd[0] to vd[7]. The first row 702 is comprised of placeholders to indicate the 8 elements. Below the first row 702 are 8 different shuffle operations in OB mode as indicated by the content of destination
10 vector register, vd, for each row 704 to 718. These shuffle operations in OB mode are illustrated in Figures 8A through 8H.

 Figure 8A illustrates a block diagram of a shuffle operation, which converts four unsigned upper bytes (i.e., 8 bits) in a source register to four 16-
15 bit halves in a destination register. This shuffle operation, represented by mnemonic UPUH.OB, selects the upper 4 8-bit elements in an exemplary vector register, vs. The selected elements vs[4], vs[5], vs[6], and vs[7] are replicated into destination elements vd[0], vd[2], vd[4], and vd[6], respectively. The odd elements of the destination vector register vd[1], vd[3], vd[5], and
20 vd[7] are zeroed.

 Figure 8B illustrates a block diagram of a shuffle operation, which converts a vector of unsigned low 4 bytes in a register to 16-bit halves. This shuffle operation, represented by mnemonic UPUL.OB, selects the lower 4 8-
25 bit elements in an exemplary vector register, vs. The selected elements vs[0], vs[1], vs[2], and vs[3] are replicated into destination elements vd[0], vd[2],

vd[4], and vd[6], respectively. The odd elements of the destination vector register vd[1], vd[3], vd[5], and vd[7] are zeroed.

Figure 8C illustrates a block diagram of a shuffle operation, which
5 converts a vector of signed upper 4 bytes in a register to 16-bit halves. This shuffle operation, represented by mnemonic UPSH.OB, selects the upper 4 8-bit elements in an exemplary vector register, vs. The selected elements vs[4], vs[5], vs[6], and vs[7] are replicated into destination elements vd[0], vd[2], vd[4], and vd[6], respectively. The odd elements of the destination vector
10 register vd[1], vd[3], vd[5], and vd[7] replicates the sign bits of the selected elements vs[4], vs[5], vs[6], and vs[7], respectively.

Figure 8D illustrates a block diagram of a shuffle operation, which
converts a vector of signed low 4 bytes in a register to 16-bit halves. This
15 shuffle operation, represented by mnemonic UPSL.OB, selects the lower 4 8-bit elements in an exemplary vector register, vs. The selected elements vs[0], vs[1], vs[2], and vs[3] are replicated into destination elements vd[0], vd[2], vd[4], and vd[6], respectively. The odd elements of the destination vector register vd[1], vd[3], vd[5], and vd[7] replicates the sign bits of the selected
20 elements vs[0], vs[1], vs[2], and vs[3], respectively.

Figure 8E illustrates a block diagram of a shuffle operation, which
replicates the odd elements of 8 8-bit elements from each of two source
registers into 8 elements in a destination vector register. This shuffle
25 operation, represented by an exemplary mnemonic PACH.OB, selects the odd elements of 8 8-bit elements in exemplary source vector registers, vs and vt. The elements selected from vs, namely vs[1], vs[3], vs[5], and vs[7] are

replicated into destination elements vd[4], vd[5], vd[6], and vd[7], respectively. The elements vt[1], vt[3], vt[5], and vt[7] from the vector register vt are replicated into destination elements vd[0], vd[1], vd[2], and vd[3], respectively.

- 5 Figure 8F illustrates a block diagram of a shuffle operation, which replicates the even elements of 8 8-bit elements from each of two source registers into 8 elements in a destination vector register. This shuffle operation, represented by an exemplary mnemonic PACL.OB, selects the even elements of 8 8-bit elements in exemplary source vector registers, vs and vt.
- 10 The elements selected from vs, namely vs[0], vs[2], vs[4], and vs[8] are replicated into destination elements vd[4], vd[5], vd[6], and vd[7], respectively. The elements vt[0], vt[2], vt[4], and vt[6] from the vector register vt are replicated into destination elements vd[0], vd[1], vd[2], and vd[3], respectively.

- 15 Figure 8G illustrates a block diagram of a shuffle operation, which replicates the upper 4 elements of 8 8-bit elements from each of two source registers into 8 elements in a destination vector register. This shuffle operation, represented by an exemplary mnemonic MIXH.OB, selects the upper 4 elements of 8 8-bit elements in exemplary source vector registers, vs
- 20 and vt. The elements selected from vs, namely vs[4], vs[5], vs[6], and vs[7] are replicated into the odd elements of the destination vector register, namely vd[1], vd[3], vd[5], and vd[7], respectively. The elements vt[4], vt[5], vt[6], and vt[7] from the vector register vt are replicated into the even elements of the destination elements vd[0], vd[2], vd[4], and vd[6], respectively.

25

Figure 8H illustrates a block diagram of a shuffle operation, which replicates the lower 4 elements of 8 8-bit elements from each of two source

registers into 8 elements in a destination vector register. This shuffle operation, represented by an exemplary mnemonic MIXL.OB, selects the lower 4 elements of 8 8-bit elements in exemplary source vector registers, vs and vt. The elements selected from vs, namely vs[0], vs[1], vs[2], and vs[3] are replicated into the odd elements of the destination vector register, namely vd[1], vd[3], vd[5], and vd[7], respectively. The elements vt[0], vt[1], vt[2], and vt[3] from the vector register vt are replicated into the even elements of the destination elements vd[0], vd[2], vd[4], and vd[6], respectively.

A shuffle instruction operating in QH mode generates a new vector of elements for two types of operations. The first type of operation creates a vector of new data sizes by converting data sizes between 16-bit elements and 32-bit elements in a vector. The second type creates a new vector of elements drawn from two other vectors. The present exemplary data type conversion operations enable a larger range of computational data format than their storage format, such as 32 bit computation on 16 bit numbers. In addition, the present embodiment operations allow conversion of a data set from a smaller range format to a larger range format or vice versa as between 16 and 32 bit data.

Figure 9 illustrates shuffle operations for ordering 16-bit elements in a 64-bit doubleword. Each row represents the destination vector register, vd, comprised of 4 elements, vd[0] to vd[7]. The first row 902 is comprised of placeholders to indicate the 4 elements. Below the first row 902 are 4 different shuffle operations in QH mode as indicated by the content of destination vector register, vd, for each row 904 to 918. These shuffle operations in QH mode are illustrated in Figures 10A through 10H.

Figure 10A illustrates a block diagram of a shuffle operation, which replicates the upper 2 elements of 4 16-bit elements from each of two source registers into 4 elements in a destination vector register. This shuffle operation, represented by an exemplary mnemonic MIXH.QH, selects the upper 2 elements of 4 16-bit elements in exemplary source vector registers, *vs* and *vt*. The elements selected from *vs*, namely *vs*[2] and *vs*[3] are replicated into the odd elements of the destination vector register, namely *vd*[1] and *vd*[3], respectively. The elements *vt*[2] and *vt*[3] from the vector register *vt* are replicated into the even elements of the destination elements *vd*[0] and *vd*[2], respectively.

Figure 10B illustrates a block diagram of a shuffle operation, which replicates the lower 2 elements of 4 16-bit elements from each of two source registers into 4 elements in a destination vector register. This shuffle operation, represented by an exemplary mnemonic MIXL.QH, selects the lower 2 elements of 4 16-bit elements in exemplary source vector registers, *vs* and *vt*. The elements selected from *vs*, namely *vs*[0] and *vs*[1] are replicated into the odd elements of the destination vector register, namely *vd*[1] and *vd*[3], respectively. The elements *vt*[0] and *vt*[1] from the vector register *vt* are replicated into the even elements of the destination elements *vd*[0] and *vd*[2], respectively.

Figure 10C illustrates a block diagram of a shuffle operation, which replicates 2 odd elements of 4 16-bit elements from each of two source registers into 4 elements in a destination vector register. This shuffle operation, represented by an exemplary mnemonic PACH.QH, selects the 2

odd elements of 4 16-bit elements in exemplary source vector registers, *vs* and *vt*. The elements selected from *vs*, namely *vs*[1] and *vs*[3] are replicated into the upper 2 elements of the destination vector register, namely *vd*[2] and *vd*[3], respectively. The elements *vt*[1] and *vt*[3] from the vector register *vt* are replicated into the lower 2 elements of the destination elements *vd*[0] and *vd*[1], respectively.

Figure 10D illustrates a block diagram of a shuffle operation, which replicates 2 even elements of 4 16-bit elements from each of two source registers into 4 elements in a destination vector register. This shuffle operation, represented by an exemplary mnemonic *PACL.QH*, selects the 2 even elements of 4 16-bit elements in exemplary source vector registers, *vs* and *vt*. The elements selected from *vs*, namely *vs*[0] and *vs*[2] are replicated into the upper 2 elements of the destination vector register, namely *vd*[2] and *vd*[3], respectively. The elements *vt*[0] and *vt*[2] from the vector register *vt* are replicated into the lower 2 elements of the destination elements *vd*[0] and *vd*[1], respectively.

Figure 10E illustrates a block diagram of a shuffle operation, which replicates even elements from one source register and odd elements from another source register into a destination vector register. This shuffle operation, represented by an exemplary mnemonic *BFLA.QH*, selects the 2 even elements of 4 16-bit elements from an exemplary source vector register, *vs*. The shuffle operation also selects the 2 odd elements of 4 16-bit elements from another exemplary source vector register, *vt*. The even elements selected from *vs*, namely *vs*[0] and *vs*[2] are replicated into the 2 odd elements of the destination vector register, namely *vd*[1] and *vd*[3], respectively. The

odd elements $vt[1]$ and $vt[3]$ from the vector register vt are replicated into the 2 even elements of the destination elements $vd[0]$ and $vd[1]$, respectively.

Figure 10F illustrates a block diagram of a shuffle operation, which
5 replicates even elements from one source register and odd elements from
another source register into a destination vector register. This shuffle
operation, represented by an exemplary mnemonic BFLB.QH, selects the 2
even elements of 4 16-bit elements from an exemplary source vector register,
 vs . The shuffle operation also selects the 2 odd elements of 4 16-bit elements
10 from another exemplary source vector register, vt . The even elements
selected from vs , namely $vs[0]$ and $vs[2]$ are replicated into the 2 odd elements
of the destination vector register in reverse order, namely $vd[3]$ and $vd[1]$,
respectively. The odd elements $vt[1]$ and $vt[3]$ from the vector register vt are
replicated into the 2 even elements of the destination elements in reverse
15 order, namely $vd[0]$ and $vd[1]$, respectively.

Figure 10G illustrates a block diagram of a shuffle operation, which
replicates the upper 2 elements of 4 16-bit elements from each of two source
registers into a destination vector register. This shuffle operation,
20 represented by an exemplary mnemonic REPA.QH, selects the upper 2
elements of 4 16-bit elements in exemplary source vector registers, vs and vt .
The upper elements selected from vs , namely $vs[2]$ and $vs[3]$ are replicated
into the upper elements of the destination vector register, namely $vd[2]$ and
 $vd[3]$, respectively. The upper elements $vt[2]$ and $vt[3]$ from the vector register
25 vt are replicated into the lower elements of the destination elements $vd[0]$
and $vd[1]$, respectively.

Figure 10H illustrates a block diagram of a shuffle operation, which replicates the lower 2 elements of 4 16-bit elements from each of two source registers into a destination vector register. This shuffle operation, represented by an exemplary mnemonic `REPB.QH`, selects the lower 2 elements of 4 16-bit elements in exemplary source vector registers, `vs` and `vt`. The lower elements selected from `vs`, namely `vs[0]` and `vs[1]` are replicated into the upper elements of the destination vector register, namely `vd[2]` and `vd[3]`, respectively. The lower elements `vt[0]` and `vt[1]` from the vector register `vt` are replicated into the lower elements of the destination elements `vd[0]` and `vd[2]`, respectively.

The shuffle instructions allow more efficient SIMD vector operations. First, the shuffle operation creates a vector of new data sizes by converting between 8-bit elements and 16-bit elements in a vector. These data type conversions enable a larger range of computational data format than their storage format, such as 16 bit computation on 8 bit numbers. For example, these operations allow conversion of a data set from a smaller range format to a larger range format or vice versa as between 8 and 16 bit audio or video data.

Second, the shuffle operations are also useful in interleaving and deinterleaving data. For example, some applications store multiple channel data in separate arrays, or interleaved in a single array. These applications typically require interleaving or deinterleaving the multiple channels. In these applications, separate R, G, B, A byte arrays may be converted into an interleaved RGBA array by the following series of shuffle instructions:

```
MIXLOB RGL, R, G          ; RGRGRGRG
```

```

MIXL.OB BAL, B, A      ; BABABABA
MIXH.OB RGH, R, G      ; RGRGRGRG
MIXH.OB BAH, B, A      ; BABABABA
MIXL.QS RGBALL, RGL, BAL ; RGBARGBA
5  MIXH.QS RGBALH, RGL, BAL ; RGBARGBA
MIXL.QS RGBAHL, RGH, BAH ; RGBARGBA
MIXH.QS RGBAAH, RGH, BAH; RGBARGBA

```

Conversely, an interleaved RGBA array may be deinterleaved into separate R, G, B, and A arrays by the following series of shuffle instructions:

```

10  PACL.OB  GA0GA1, RGBA0, RGBA1
    PACH.OB  RB0RB1, RGBA0, RGBA1
    PACL.OB  GA2GA3, RGBA2, RGBA3
    PACH.OB  RB2RB3, RGBA2, RGBA3
15  PACL.OB  A0A1A2A3, GA0GA1, GA2GA3
    PACH.OB  G0G1G2G3, GA0GA1, GA2GA3
    PACL.OB  B0B1B2B3, RB0RB1, RB2RB3
    PACH.OB  R0R1R2R3, RB0RB1, RB2RB3

```

20 Third, some algorithms operate on 2 dimensional arrays of data such as images. Such an array typically orders the elements of the array in a major axis, where the elements are consecutive, and a minor axis, where the elements are separated by the size of the major axis. Often, a transpose operation is performed on the 2 dimensional array by converting the major axis to minor axis and vice versa. A common example is a discrete cosine transformation (DCT) requiring transposing 8x8 block of array. In this example, the 8x8 block of array consists of following elements:

		d0	d1	d2	d3	d4	d5	d6	d7
30	s0	A0	B0	C0	D0	E0	F0	G0	H0
	s1	A1	B1	C1	D1	E1	F1	G1	H1
	s2	A2	B2	C2	D2	E2	F2	G2	H2
	s3	A3	B3	C3	D3	E3	F3	G3	H3
	s4	A4	B4	C4	D4	E4	F4	G4	H4
35	s5	A5	B5	C5	D5	E5	F5	G5	H5
	s6	A6	B6	C6	D6	E6	F6	G6	H6
	s7	A7	B7	C7	D7	E7	F7	G7	H7

The present invention can transpose the 8x8 transpose in OB mode in 24 instructions, of which 12 are shown as follows:

5	MIXH.OB t0, s0, s1	A0 A1 B0 B1 C0 C1 D0 D1
	MIXH.OB t1, s2, s3	A2 A3 B2 B3 C2 C3 D2 D3
	MIXH.OB t2, s4, s5	A4 A5 B4 B5 C4 C5 D4 D5
	MIXH.OB t3, s6, s7	A6 A7 B6 B7 C6 C7 D6 D7
	MIXH.QH u0, t0, t1	A0 A1 A2 A3 B0 B1 B2 B3
	MIXH.QH u1, t2, t3	A4 A5 A6 A7 B4 B5 B6 B7
10	MIXH.QH u2, t0, t1	C0 C1 C2 C3 D0 D1 D2 D3
	MIXH.QH u3, t2, t3	C4 C5 C6 C7 D4 D5 D6 D7
	REPA.QH d0, u0, u1	A0 A1 A2 A3 A4 A5 A6 A7
	REP.B.QH d1, u0, u1	B0 B1 B2 B3 B4 B5 B6 B7
	REPA.QH d2, u2, u3	C0 C1 C2 C3 C4 C5 C6 C7
15	REP.B.QH d3, u2, u3	D0 D1 D2 D3 D4 D5 D6 D7
	MIXL.OB t0, s0, s1	E0 E1 F0 F1 G0 G1 H0 H1
	MIXL.OB t1, s2, s3	E2 E3 F2 F3 G2 G3 H2 H3
	MIXL.OB t2, s4, s5	E4 E5 F4 F5 G4 G5 H4 H5
20	MIXL.OB t3, s6, s7	E6 E7 F6 F7 G6 G7 H6 H7
	MIXL.QH u0, t0, t1	E0 E1 E2 E3 F0 F1 F2 F3
	MIXL.QH u1, t2, t3	E4 E5 E6 E7 F4 F5 F6 F7
	MIXL.QH u2, t0, t1	G0 G1 G2 G3 H0 H1 H2 H3
	MIXL.QH u3, t2, t3	G4 G5 G6 G7 H4 H5 H6 H7
25	REPA.QH d0, u0, u1	E0 E1 E2 E3 E4 E5 E6 E7
	REP.B.QH d1, u0, u1	F0 F1 F2 F3 F4 F5 F6 F7
	REPA.QH d2, u2, u3	G0 G1 G2 G3 G4 G5 G6 G7
	REP.B.QH d3, u2, u3	H0 H1 H2 H3 H4 H5 H6 H7

30 In another example, an exemplary 4x4 array block consists of following elements:

		d0	d1	d2	d3
35	s0	A	B	C	D
	s1	E	F	G	H
	s2	I	J	K	L
	s3	M	N	O	P

A transpose operation of the 4x4 array block in QH mode uses 8 shuffle instructions as follows:

40	MIXH.QH t0, s0, s1	A E B F
	MIXH.QH t1, s2, s3	I M J N

REPA.QH d0, t0, t1	A E I M
REPB.QH d1, t0, t1	B F J N
MIXL.QH t0, s0, s1	C G D H
MIXL.QH t1, s2, s3	K O L P
REPA.QH d2, t0, t1	C G K O
REPB.QH d3, t0, t1	D H L P

5

10

15

The shuffle instructions such as BFLA and BFLB allow reversing the order of elements in an array, in pairs or groups of 4. Larger groups can be reordered by memory or register address because they are a multiple of 64 bit elements. Inverting the order of a large array can be accomplished by inverting each vector of 4 elements with BFLB and loading from or storing each doubleword to the mirrored address in the array. Similarly, a butterfly on a large array can be assembled from double word addressing and BFLA or BFLB operations on the addressed doublewords.

20

The present invention thus provides a method for providing element alignment and ordering for SIMD processing. While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not be construed as being limited by such embodiments, but rather construed according to the claims below.

CLAIMS

What is claimed is:

1. In a computer system including a processor having a plurality of registers, a method for generating an aligned vector of first width from two
5 second width vectors for single instruction multiple data (SIMD) processing, comprising the steps of:
loading a first vector from a memory unit into a first register, wherein the first vector contains a first byte of an aligned vector to be generated;
loading a second vector from the memory unit into a second register;
10 determining a starting byte in the first register wherein the starting byte specifies the first byte of an aligned vector;
extracting a first width vector from the first register and the second register beginning from the first bit in the first byte of the first register continuing through the bits in the second register; and
15 replicating the extracted first width vector into a third register such that the third register contains a plurality of elements aligned for SIMD processing.
2. The method as recited in Claim 1 further comprising the step of
20 storing the aligned vector in the third register to the memory unit.
3. The method as recited in Claim 1, wherein the first width and second width are each 64 bits.
- 25 4. The method as recited in Claim 3, wherein the third register is comprised of 8 8-bit elements.

5. The method as recited in Claim 3, wherein the third register is comprised of 4 16-bit elements.

6. The method as recited in Claim 1, wherein the starting byte is
5 specified as a constant in an alignment instruction.

7. The method as recited in Claim 1, wherein the starting byte is specified as a variable in a register in an alignment instruction.

10 8. The method as recited in Claim 1, wherein the first vector and the second vector are in contiguous location in the memory unit.

9. The method as recited in Claim 1, wherein the processor operates in a big-endian byte ordering mode.

15

10. The method as recited in Claim 1, wherein the processor operates in a little-endian byte ordering mode.

11. In a computer system including a processor having a plurality of
20 registers, a method for generating an ordered set of elements in an N-bit vector from two sets of elements in two N-bit vectors for single instruction multiple data (SIMD) vector processing, said method comprising the steps of:
loading a first vector from a memory unit into a first register;
loading a second vector from the memory unit into a second register;
25 selecting a subset of elements from the first register and the second register; and

replicating the elements from the subset into the elements in the third register in a particular order suitable for subsequent SIMD vector processing.

12. The method as recited in Claim 11 further comprising the step of
5 storing the elements in the third register to the memory unit.

13. The method as recited in Claim 11, wherein the first vector and the second vector are each comprised of 4 16-bit elements indexed from 0 to 3.

10 14. The method as recited in Claim 11, wherein the first vector and the second vector are each comprised of 8 8-bit elements indexed from 0 to 7.

15 15. The method as recited in Claim 13, wherein the subset is comprised of two elements from the first register and two elements from the second register.

16. The method as recited in Claim 14, wherein the subset is comprised of four elements from the first register and four elements from the second register.

20

17. The method as recited in Claim 13, wherein the subset is comprised of the elements 2 and 3 from the first register and the elements 2 and 3 from the second register.

25 18. The method as recited in Claim 17, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 2 of the second register;

the element 1 replicated from the element 2 of the first register;
the element 2 replicated from the element 3 of the second register; and
the element 3 replicated from the element 3 of the first register.

5 19. The method as recited in Claim 13, wherein the subset is
comprised of the elements 0 and 1 from the first register and the elements 0
and 1 from the second register.

 20. The method as recited in Claim 19, wherein the particular order
10 of the elements in the third register comprises:

the element 0 replicated from the element 0 of the second register;
the element 1 replicated from the element 0 of the first register;
the element 2 replicated from the element 1 of the second register; and
the element 3 replicated from the element 1 of the first register.

15

 21. The method as recited in Claim 13, wherein the subset is
comprised of the elements 1 and 3 from the first register and the elements 1
and 3 from the second register.

20 22. The method as recited in Claim 21, wherein the particular order
of the elements in the third register comprises:

the element 0 replicated from the element 1 of the second register;
the element 1 replicated from the element 3 of the second register;
the element 2 replicated from the element 1 of the first register; and
25 the element 3 replicated from the element 3 of the first register.

23. The method as recited in Claim 13, wherein the subset is comprised of the elements 0 and 2 from the first register and the elements 0 and 2 from the second register.

5 24. The method as recited in Claim 23, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 0 of the second register;
the element 1 replicated from the element 2 of the second register;
the element 2 replicated from the element 0 of the first register; and
10 the element 3 replicated from the element 2 of the first register.

25. The method as recited in Claim 13, wherein the subset is comprised of the elements 0 and 2 from the first register and the elements 1 and 3 from the second register.

15 26. The method as recited in Claim 25, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 1 of the second register;
the element 1 replicated from the element 0 of the first register;
20 the element 2 replicated from the element 3 of the second register; and
the element 3 replicated from the element 2 of the first register.

27. The method as recited in Claim 13, wherein the subset is comprised of the elements 0 and 2 from the first register and the elements 1
25 and 3 from the second register.

28. The method as recited in Claim 27, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 3 of the second register;
the element 1 replicated from the element 2 of the first register;
5 the element 2 replicated from the element 1 of the second register; and
the element 3 replicated from the element 0 of the first register.

29. The method as recited in Claim 13, wherein the subset is comprised of the elements 2 and 3 from the first register and the elements 2
10 and 3 from the second register.

30. The method as recited in Claim 29, wherein particular order of the elements in the third register comprises:

the element 0 replicated from the element 2 of the second register;
15 the element 1 replicated from the element 3 of the second register;
the element 2 replicated from the element 2 of the first register; and
the element 3 replicated from the element 3 of the first register.

31. The method as recited in Claim 13, wherein the subset is comprised of the elements 0 and 2 from the first register and the elements 0
20 and 1 from the second register.

32. The method as recited in Claim 31, wherein the particular order of the elements in the third register comprises:

25 the element 0 replicated from the element 0 of the second register;
the element 1 replicated from the element 1 of the second register;
the element 2 replicated from the element 0 of the first register; and

the element 3 replicated from the element 2 of the first register.

33. The method as recited in Claim 14, wherein the subset is comprised of the elements 1, 3, 5, and 7 from the first register and the
5 elements 1, 3, 5, and 7 from the second register.

34. The method as recited in Claim 33, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 1 of the second register;
10 the element 1 replicated from the element 3 of the second register;
the element 2 replicated from the element 5 of the second register;
the element 3 replicated from the element 7 of the second register;
the element 4 replicated from the element 1 of the first register;
the element 5 replicated from the element 3 of the first register;
15 the element 6 replicated from the element 5 of the first register; and
the element 7 replicated from the element 7 of the first register.

35. The method as recited in Claim 14, wherein the subset is comprised of the elements 0, 2, 4, and 6 from the first register and the
20 elements 0, 2, 4, and 6 from the second register.

36. The method as recited in Claim 35, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 0 of the second register;
25 the element 1 replicated from the element 2 of the second register;
the element 2 replicated from the element 4 of the second register;
the element 3 replicated from the element 6 of the second register;

the element 4 replicated from the element 0 of the first register;
the element 5 replicated from the element 2 of the first register;
the element 6 replicated from the element 4 of the first register; and
the element 7 replicated from the element 6 of the first register.

5

37. The method as recited in Claim 14, wherein the subset is comprised of the elements 4, 5, 6, and 7 from the first register and the elements 4, 5, 6, and 7 from the second register.

10

38. The method as recited in Claim 37, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 4 of the second register;
the element 1 replicated from the element 4 of the first register;
the element 2 replicated from the element 5 of the second register;
the element 3 replicated from the element 5 of the first register;
the element 4 replicated from the element 6 of the second register;
the element 5 replicated from the element 6 of the first register;
the element 6 replicated from the element 7 of the second register; and
the element 7 replicated from the element 7 of the first register.

15
20

39. The method as recited in Claim 14, wherein the subset is comprised of the elements 0, 1, 2, and 3 from the first register and the elements 0, 1, 2, and 3 from the second register.

25

40. The method as recited in Claim 39, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 0 of the second register;

the element 1 replicated from the element 0 of the first register;
the element 2 replicated from the element 1 of the second register;
the element 3 replicated from the element 1 of the first register;
the element 4 replicated from the element 2 of the second register;
5 the element 5 replicated from the element 2 of the first register;
the element 6 replicated from the element 3 of the second register; and
the element 7 replicated from the element 3 of the first register.

41. The method as recited in Claim 14, wherein the subset is
10 comprised of the elements 4, 5, 6, and 7 from the first register.

42. The method as recited in Claim 41, wherein the particular order
of the elements in the third register comprises:

the element 0 replicated from the element 4 of the first register;
15 the element 2 replicated from the element 5 of the first register;
the element 4 replicated from the element 6 of the first register;
the element 6 replicated from the element 7 of the first register; and
the elements 1, 3, 5, and 7 containing a zero in all the bits.

20 43. The method as recited in Claim 14, wherein the subset is
comprised of the elements 0, 1, 2, and 3 from the first register.

44. The method as recited in Claim 43, wherein the particular order
of the elements in the third register comprises:

25 the element 0 replicated from the element 0 of the first register;
the element 2 replicated from the element 1 of the first register;
the element 4 replicated from the element 2 of the first register;

the element 6 replicated from the element 3 of the first register; and
the elements 1, 3, 5, and 7 containing a zero in all the bits.

45. The method as recited in Claim 14, wherein the subset is
5 comprised of the elements 4, 5, 6, and 7 from the first register.

46. The method as recited in Claim 45, wherein the particular order
of the elements in the third register comprises:

the element 0 replicated from the element 4 of the first register;
10 the element 1 replicating the sign bit of the element 4 of the first
register in all the bits;

the element 2 replicated from the element 5 of the first register;
the element 3 replicating the sign bit of the element 5 of the first
register in all the bits;

15 the element 4 replicated from the element 6 of the first register;
the element 5 containing the sign bit of the element 6 of the first
register in all the bits;

the element 6 replicated from the element 7 of the first register; and
the element 7 containing the sign bit of the element 7 of the first
20 register in all the bits.

47. The method as recited in Claim 14, wherein the subset is
comprised of the elements 0, 1, 2, and 3 from the first register.

25 48. The method as recited in Claim 47, wherein the particular order
of the elements in the third register comprises:

the element 0 replicated from the element 0 of the first register;

the element 1 containing the sign bits of the element 0 of the first register;

the element 2 replicated from the element 1 of the first register;

the element 3 containing the sign bits of the element 1 of the first

5 register;

the element 4 replicated from the element 2 of the first register;

the element 5 containing the sign bits of the element 2 of the first

register;

the element 6 replicated from the element 3 of the first register; and

10 the element 7 containing the sign bits of the element 3 of the first register.

ABSTRACT

The present invention provides alignment and ordering of vector elements for SIMD processing. In the alignment of vector elements for SIMD processing, one vector is loaded from a memory unit into a first register and another vector is loaded from the memory unit into a second register. The first vector contains a first byte of an aligned vector to be generated. Then, a starting byte specifying the first byte of an aligned vector is determined. Next, a vector is extracted from the first register and the second register beginning from the first bit in the first byte of the first register continuing through the bits in the second register. Finally, the extracted vector is replicated into a third register such that the third register contains a plurality of elements aligned for SIMD processing. In the ordering of vector elements for SIMD processing, a first vector is loaded from a memory unit into a first register and a second vector is loaded from the memory unit into a second register. Then, a subset of elements are selected from the first register and the second register. The elements from the subset are then replicated into the elements in the third register in a particular order suitable for subsequent SIMD vector processing.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Van Hook *et al*

Appl. No.: To be assigned

Filed: Herewith

For: **Alignment and Ordering of
Vector Elements for Single
Instruction Multiple Data
Processing**

Art Unit: To be assigned

Examiner: To be assigned

Atty. Docket: 1778.0100002
(0055.20US)

Preliminary Amendment

Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination of the above-captioned application, Applicant submits the following Amendments and Remarks.

In the Specification:

Page 1, between lines 3 and 4, please insert the following:

--This application is a continuation of U.S. Patent Application No. 09/263,798, filed March 5, 1999, which is a continuation of U.S. Patent Application No. 08/947,649, filed October 9, 1997, now U.S. Patent No. 5,933,650, issued August 3, 1999.--

In the Claims:

Please cancel claims 2-48 without prejudice or disclaimer.

Remarks

Upon entry of the foregoing amendments, claim 1 is pending in the application. Claims 2-48 are sought to be canceled without prejudice or disclaimer. The above amendments are to matters of form only and their entry is respectfully requested. These changes are believed to introduce no new matter, and their entry is respectfully requested.

The Examiner is invited to telephone the undersigned representative if he believes that an interview might be useful for any reason.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



Michael B. Ray
Attorney for Applicant
Registration No. 33,997

Date: 9/15/00

1100 New York Avenue, N.W.
Suite 600
Washington, D.C. 20005-3934
(202) 371-2600

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Timothy J. Van Hook *et al.*

Appl. No. 09/662,832

Filed: September 15, 2000

For: **Alignment and Ordering of
Vector Elements For Single
Instruction Multiple Data
Processing**

Confirmation No.: (to be assigned)

Art Unit: 2183

Examiner: (to be assigned)

Atty. Docket: 1778.0100002
(0055.20US)

Second Preliminary Amendment

Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination of the above-captioned application, Applicants submit the following Amendment and Remarks. This Amendment is provided in the following format:

- (A) A clean version of each replacement paragraph/section/claim along with clear instructions for entry;
- (B) Starting on a separate page, appropriate remarks and arguments. 37 C.F.R. § 1.111 and MPEP 714; and
- (C) Starting on a separate page, a marked-up version entitled: "Version with markings to show changes made."

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent

abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments

In the Claims:

Please add the following new claims:

49. (New) A method for generating an aligned vector from two source vectors for single instruction multiple data (SIMD) processing, comprising the steps of:

- (1) loading a first source vector into a first register;
- (2) loading a second source vector into a second register;
- (3) reading a first plurality of elements from said first register and a second plurality of elements from said second register; and
- (4) writing said first plurality of elements and said second plurality of elements into a third register in a particular order to produce a target vector having a plurality of elements aligned for SIMD processing.

50. (New) The method as recited in claim 49, wherein said writing step comprises:

writing even-numbered, lower elements of said first register to said third register;

and

writing sign bits of odd-numbered, lower elements of said first register to said third register.

51. (New) The method as recited in claim 49, wherein said writing step comprises:

writing even-numbered, upper elements of said first register to said third register;

and

writing sign bits of odd-numbered, upper elements of said first register to said third register.

52. (New) A method for generating an ordered set of elements in a target vector from elements in a first source vector and a second source vector for single instruction multiple data (SIMD) vector processing, comprising the steps of:

- (1) loading the first source vector into a first register;
- (2) loading the second source vector into a second register;
- (3) selecting a first subset of elements from said first register, said first subset comprising any one of the following groups of elements from the first source vector: odd elements, even elements, lower elements and upper elements; and

(4) selecting a second subset of elements from said second register, said second subset comprising any one of the following groups of elements from the second source vector: odd elements, even elements, lower elements and upper elements.

53. (New) The method of claim 52, further comprising the step of:

(5) writing said first and said second subset of elements into a third register to facilitate a particular SIMD vector processing operation, said first subset being written into any one of the following groups of elements in said third register: upper elements, odd elements, and odd elements in reverse order, and said second subset being written into any one of the following groups of elements in said third register: lower elements, even elements, and even elements in reverse order, wherein elements written into said third register comprise the target vector.

Remarks

Upon entry of the foregoing amendment, claims 1 and 49-53 are pending in the application, with 1, 49 and 52 being the independent claims. New claims 49-53 are sought to be added. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Consideration of all pending claims is respectfully solicited. The Examiner is invited to telephone the undersigned representative if he believes that an interview might be useful for any reason.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



Michael B. Ray
Attorney for Applicants
Registration No. 33,997

Date: 4/9/01

1100 New York Avenue, N.W., Suite 600
Washington, D.C. 20005-3934
(202) 371-2600

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Timothy J. Van Hook *et al*

Appl. No. 09/662,832

Filed: September, 15, 2000

For: **Alignment and Ordering of
Vector Elements for Single
Instruction Multiple Data
Processing**

Confirmation No.: 2552

Art Unit: 2183

Examiner: Pan, D.

Atty. Docket: 1778.0100002 (0055.20US)

Amendment And Reply Under 37 C.F.R. § 1.111

Commissioner for Patents
Washington, D.C. 20231

Sir:

In reply to the Office Action dated August 24, 2001, (PTO Prosecution File Wrapper Paper No. 8), Applicants submit the following Amendment and Remarks. This Amendment is provided in the following format:

- (A) A clean version of each replacement paragraph/section/claim along with clear instructions for entry;
- (B) Starting on a separate page, appropriate remarks and arguments. 37 C.F.R. § 1.111 and MPEP 714; and
- (C) Starting on a separate page, a marked-up version entitled: "Version with markings to show changes made."

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R.

§ 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments

In the Claims:

Please substitute the following claim 1 for the pending claim 1:

1. (once amended) In a computer system including a processor having a plurality of registers, a method for generating an aligned vector of first width from two second width vectors for single instruction multiple data (SIMD) processing, comprising the steps of:

loading a first vector from a memory unit into a first register, wherein the first vector contains a first byte of the aligned vector to be generated;

loading a second vector from the memory unit into a second register;

determining a starting byte in the first register wherein the starting byte specifies the first byte of the aligned vector;

extracting the aligned vector from the first register and the second register beginning from the first bit in the starting byte of the first register continuing through bits in the second register; and

replicating the aligned vector into a third register such that the third register contains a plurality of elements aligned for SIMD processing.

Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1 and 49-53 are pending in the application, with claims 1, 49, and 52 being the independent claims. Claim 1 is sought to be amended. No new matter is embraced by this amendment and its entry is respectfully solicited. Based on this amendment and the remarks set forth below, it is respectfully requested that the Examiner reconsider and withdraw all outstanding objections and rejections.

The Applicant would like to thank the Examiner for the interview on January 10, 2002. During that interview the differences between the claimed invention and U.S. Patent No. 5,887,183 to Agarwal *et al.* were discussed. The Examiner acknowledged the differences and indicated that he would look into the case in the next response.

Description of the Invention

The present invention is directed to a method of processing instructions for Single Instruction/Multiple Data (hereinafter, "SIMD") processing. The method includes steps of aligning and ordering vector elements for SIMD processing. To align the vectors for SIMD processing, a first vector is loaded into a first register, and a second vector is loaded into a second register. A first width vector is extracted from the first register and the second register. The resulting extracted vector starts from a first bit of a starting byte in the first width vector and continues through bits of the second width vector. The extracted vector

is then replicated into a third register. To order elements for SIMD processing, a first subset of elements (which may include odd bytes, even bytes, upper bytes, lower bytes or any combination of these) is chosen from the first register and a second subset of elements (which may include odd bytes, even bytes, upper bytes, lower bytes or any combination of these) is chosen from the second register. The chosen elements are replicated into the third register.

An advantage of the present invention is that it allows for faster parallel processing of instructions to be used for SIMD processing. Furthermore, the present invention allows processing, for example, of 64-bit vectors containing different size elements (e.g., a 64-bit vector may contain eight 8-bit elements, four 16-bit elements, two 32-bit elements or one 64-bit element). The vectors are processed according to the element subdivision within each vector register.

Rejections under 35 U.S.C. § 112

In the Office Action dated August 24, 2001, the Examiner has rejected claim 1 under 35 USC § 112, ¶ 2, as being indefinite for failing particularly point out and distinctly claim the subject matter which the Applicants' regard as their invention. Claim 1 is sought to be amended to correct this minor antecedent basis error. In view of this amendment, Applicants respectfully request that this rejection be reconsidered and withdrawn.

Rejections under 35 U.S.C. § 103

In the Office Action dated August 24, 2001, the Examiner has rejected claims 1, 49, and 52 under 35 USC § 103(a) as being unpatentable over U.S. Patent No. 5,887,183 to Agarwal *et al.* in view of U.S. Patent No. 5,922,066 to Cho *et al.*.

With respect to claim 1, the Examiner states that all of the steps of claim 1 except the last the step of replicating of the first width vector into a third register are described by the Agarwal reference and the step of replicating is described by the Cho reference. With respect to claim 49, the Examiner gives a similar rejection under 35 USC § 103(a) and states that even though the Agarwal reference does not specifically describe the writing step of claim 49, the Cho reference provides such step. With respect to claim 52, the Examiner states that the Agarwal reference does not specifically describe the step of selecting the first subset of elements and the step of selecting the second subset of elements, however, the Examiner states that Cho reference provides such steps. The Examiner states that it would have been obvious to one of ordinary skill in the art to combine the two references to produce the claimed subject matter of claim 52.

The Examiner's rejections are respectfully traversed for the reasons set forth below, and the Examiner is respectfully requested to reconsider and withdraw any objections or rejections with respect to claims 1, 49, and 52.

Agarwal describes a method and a system for loading and storing vectors (having a plurality of elements) in a plurality of modes. The vectors are stored in an input storage area, then the elements of the vectors are transferred from the input storage area into a vector

register interface unit. From the vector interface unit, the vector elements are transferred to addressable locations in a preselected pattern in the output storage area. See Agarwal at col. 9, lines 66-67; col. 10, line 1-5; col. 10, lines 46-53; and FIGS. 4A and 4B. The vector elements may be stored in a designated pattern (where such pattern has alternating real and imaginary elements) in the input storage area. Furthermore, the vectors elements may be separated into real and imaginary elements in the output storage area.

Cho describes a system and a method for aligning data for load and/or store instructions. The system of Cho is capable of rotating and shifting data for arithmetic logic instructions. Cho describes an aligner that is adapted to align data as required for load/store instructions and to shift data elements within an operand as required for a shift instruction. Cho uses the same circuit to perform two operations, thus, reducing an overall circuit size. Cho provides for a SIMD processor including an instruction fetch unit, dual instruction decoders, a vector register file, a scalar register file and dual execution units capable of operating in parallel. The instruction decoder of Cho decodes the instructions, which the execution units execute. Such instructions may be to add, subtract, divide or multiply source operands.

The system of Cho is capable of loading/storing data and shifting the data within an operand (which requires a logical or arithmetic operation, left or right shift, rotate or change of position of the elements in the operand). The instruction fetch unit fetches up to two instructions for each of the decoders per each cycle to be processed. The decoders process and pass each instruction onto either the vector or scalar register file. The vector register file contains 64 32-byte vector registers that are organized into two banks of 32 vector registers.

The scalar register file contains 32 32-bit scalar register files, where each register file contains a single 8-bit, 16-bit, or 32-bit value. After processing, the results are forwarded into execution units containing aligners. The execution units perform such functions as load, store and data move operations. The aligner is used in the load and store operations performed by the execution units. For example, for an unaligned load operation, the execution unit requests two data vectors from the memory system, which are two 32-byte data vectors, and a resultant vector is constructed from the two. For an unaligned store, the aligner rotates the data elements in the data storage so that the elements are in their correct positions for storage in two cache lines in the memory system. The aligner has an input select circuit, an element select circuit and a rotation circuit. For data element shifting or rotating, the input select circuit selects one vector operand and another operand, which may be a vector or a scalar, and shifts them into a resultant vector, when the first vector operand is shifted. The shifting and rotating are performed by the aligner include shifting elements by the N byte size elements, where N is an integer representing the number of elements to be shifted or rotated See Cho at col. 6, lines 18-39.

Claim 1

Claim 1 recites the steps of:

- loading a first vector from a memory unit into a first register, wherein the first vector contains a first byte of the aligned vector to be generated;
- loading a second vector from the memory unit into a second register;
- determining a starting byte in the first register wherein the starting byte specifies the first byte of the aligned vector;

extracting the aligned vector from the first register and the second register beginning from the first bit in the starting byte of the first register continuing through bits in the second register; and
replicating the aligned vector into a third register such that the third register contains a plurality of elements aligned for SIMD processing.

As indicated above, the Examiner has acknowledged that Agarwal does not teach the replicating step. In addition, Agarwal does not teach the steps of loading a second vector into a second register, determining a starting byte and extracting an aligned vector.

With respect to the loading step, Agarwal loads only a first vector (i.e., from vector register interface unit 216) into one or two registers (i.e., in vector register array 238). Further, Agarwal does not teach or suggest the claimed step of determining a starting byte in a first register. Instead Agarwal, stores or loads the vectors *consecutively* as they appear either in the input storage area or load area. The vectors may be stored in different patterns, such as reverse order or separated into real and imaginary components. However, Agarwal does not determine which element is the starting byte of the first vector register.

Agarwal also does not teach or suggest the claimed step of extracting the aligned vector from first and second registers beginning with the starting byte. Agarwal merely stores or loads vector register elements to and from addressable locations in preselected patterns. For example, in Agarwal, vector elements are transferred from the vector register interface unit 216 to a vector register in vector register array 238. See FIG. 4A. However, vectors are not taken from first and second registers and no alignment is taking place in the step of writing a vector to a vector register in array 238. Thus, in Agarwal, there is no teaching or suggestion of a step of extracting.

Cho does not provide the missing features. For example, Cho does not teach or suggest at least the steps of determining, and extracting. What Cho describes is a method of shifting and rotating of elements within a vector register, where a shifting operation is performed by shifting an entire first vector operand into another vector register and shifting other elements into that vector register. See Cho at col. 6, lines 18-39. This is different from the present invention, as recited in claim 1, where elements in each vector register are selected by extracting a vector from the first vector register and the second vector register.

Therefore, neither Agarwal nor Cho teaches or suggests every element of claim 1. Furthermore, the combination of Agarwal and Cho does not provide any teaching or suggestion that would lead a person of ordinary skill in the art to create the combination of steps recited in claim 1. While Agarwal discloses a system of loading or storing vectors into registers, the vectors are already pre-aligned before they are stored or loaded. The system in Agarwal determines what type of vectors (stride-1, complex, stride-n or stride-(-1)) are to be loaded/stored and loads/stores them accordingly. Cho merely describes a system of data processing that is capable of shifting and rotating data to be used for load/store functions. The combination of Agarwal and Cho would produce a system capable of performing load and store functions of vectors and performing shift operations to align the vectors from load and store operations. However, the combination would not produce the claimed method including the steps of determining a starting byte, extracting an aligned vector and replicating the aligned vector into a third register for further SIMD processing. Accordingly, Applicants submit that the rejection of claim 1 under 35 U.S.C. §103 is

improper. Based on these remarks, it is respectfully requested that the Examiner reconsider and withdraw the rejection of claim 1.

Claim 49

Claim 49 recites the steps of loading a first source vector into a first register, loading a second source vector into a second register, reading a first plurality of elements from the first register and a second plurality of elements from the second register and writing the first and second plurality of elements into a third register. As discussed above with respect to claim 1, neither Agarwal or Cho teaches or suggests these claimed features. Accordingly, claim 49 is patentable over the combination of Agarwal and Cho for the same reasons discussed above with respect to claim 1. Reconsideration and withdrawal of the rejection of claim 49 is thus respectfully requested.

Claim 52

Claim 52 recites the following steps of loading first and second source vectors into first and second registers, respectively, selecting first subset from the first register (where the subset is selected from odd, even, lower and upper elements) and selecting a second subset from the second register (where the subset is selected from: odd, even, lower and upper elements). Agarwal does not teach or suggest selecting the subsets from each respective register. As discussed above with respect to claim 1, Agarwal describes loading and storing elements in vector registers as they originally appear. The elements might be

subdivided into real and imaginary elements or might be stored in reverse order in resulting vectors. However, claim 52 recites steps of selection of elements from first and second registers to be placed into the third register. These steps are neither taught nor suggested by Agarwal.

As discussed above with respect to claim 1, neither Agarwal or Cho teaches or suggests these claimed features. Accordingly, claim 52 is patentable over the combination of Agarwal and Cho for the same reasons discussed above with respect to claim 1. Reconsideration and withdrawal of the rejection of claim 52 is thus respectfully requested.

Other Matters

The Examiner has rejected the claims 1, 49, and 52 under the doctrine of non-statutory double patenting. To accommodate this rejection, Applicant's are submitting herewith a properly executed terminal disclaimer in accordance with 37 CFR § 1.321(c). In view of this terminal disclaimer, reconsideration and withdrawal of this rejection is respectfully requested.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicant(s) therefore respectfully request(s) that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicant(s) believe that a full and complete reply has been made to the

outstanding Office Action and, as such, the present application is in condition for allowance.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

A handwritten signature in black ink, appearing to read "MB Ray", enclosed within a large, loopy circular flourish.

Michael B. Ray
Attorney for Applicants
Registration No. 33,997

Date: 1/24/01
1100 New York Avenue, N.W.
Suite 600
Washington, D.C. 20005-3934
(202) 371-2600

Version with markings to show changes made

1. (once amended) In a computer system including a processor having a plurality of registers, a method for generating an aligned vector of first width from two second width vectors for single instruction multiple data (SIMD) processing, comprising the steps of:

loading a first vector from a memory unit into a first register, wherein the first vector contains a first byte of [an] the aligned vector to be generated;

loading a second vector from the memory unit into a second register;

determining a starting byte in the first register wherein the starting byte specifies the first byte of [an] the aligned vector;

extracting [a first width] the aligned vector from the first register and the second register beginning from the first bit in the [first] starting byte of the first register continuing through [the] bits in the second register; and

replicating the [extracted first width] aligned vector into a third register such that the third register contains a plurality of elements aligned for SIMD processing.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Timothy J. van Hook *et al.*

Appl. No. 09/662,832

Filed: September 15, 2000

For: **Alignment and Ordering of
Vector Elements for Single
Instruction Multiple Data
Processing**

Confirmation No.: 2552

Art Unit: 2183

Examiner: Pan, D.

Atty. Docket: 1778.0100002
(0055.20US)

Preliminary Amendment Under 37 C.F.R. § 1.114

Commissioner for Patents
Washington, D.C. 20231

Sir:

This Preliminary Amendment is being filed along with a Request for Continued Examination Under 37 C.F.R. § 1.114. As payment of the issue fee has not yet been made, Applicants respectfully submit that filing under 37 C.F.R. § 1.114 is proper.

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

This Amendment is provided in the following format:

(A) A clean version of each replacement paragraph/section/claim along with clear instructions for entry;

(B) Starting on a separate page, appropriate remarks and arguments. 37

C.F.R. § 1.111 and MPEP 714; and

(C) Starting on a separate page, a marked-up version entitled: “Version with markings to show changes made.”

Amendments

In the Claims:

Please add the following new claims:

54.(new) The method as recited in claim 1, wherein the first width and second width are each 64 bits.

55.(new) The method as recited in claim 54, wherein the third register is comprised of eight 8-bit elements.

56.(new) The method as recited in claim 54, wherein the third register is comprised of four 16-bit elements.

57.(new) The method as recited in claim 1, wherein the starting byte is specified as a variable in a register in an alignment instruction.

58.(new) The method as recited in claim 1, wherein the first vector and the second vector are in contiguous locations in the memory unit.

59.(new) The method as recited in claim 1, wherein the processor operates in a big-endian byte ordering mode.

60.(new) The method as recited in claim 1, wherein the processor operates in a little-endian byte ordering mode.

61.(new) The method as recited in claim 1, wherein the first vector and the second vector are each composed of eight 8-bit elements indexed from 0 to 7, and wherein said extracting step comprises:

extracting elements 4, 5, 6, and 7 from the first register.

62. (new) The method as recited in claim 61, wherein said replicating step comprises:
replicating an element 0 of the third register from an element 4 of the first register;
replicating, for all bits of an element 1 of the third register, a sign bit of the element 4 of the first register;

replicating an element 2 of the third register from an element 5 of the first register;
replicating, for all bits of an element 3 of the third register, a sign bit of the element 5 of the first register;

replicating an element 4 of the third register from an element 6 of the first register;
replicating, for all bits of an element 5 of the third register, a sign bit of the element 6 of the first register;

replicating an element 6 of the third register from an element 7 of the first register;
and

replicating, for all bits of an element 7 of the third register, a sign bit of the element 7 of the first register.

63. (new) The method as recited in claim 1, wherein the first vector and the second vector are each composed of eight 8-bit elements indexed from 0 to 7, and wherein said extracting step comprises:

extracting elements 0, 1, 2 and 3 from the first register.

64. (new) The method as recited in claim 63, wherein said replicating step comprises:

replicating an element 0 of the third register from an element 0 of the first register;

replicating, for all bits of an element 1 of the third register, a sign bit of the element 0 of the first register;

replicating an element 2 of the third register from an element 1 of the first register;

replicating, for all bits of an element 3 of the third register, a sign bit of the element 1 of the first register;

replicating an element 4 of the third register from an element 2 of the first register;

replicating, for all bits of an element 5 of the third register, a sign bit of the element 2 of the first register;

replicating an element 6 of the third register from an element 3 of the first register;

and

replicating, for all bits of an element 7 of the third register, a sign bit of the element 3 of the first register.

Remarks

Upon entry of the foregoing amendment, claims 1 and 49-64 are pending in the application. Claims 1 and 49-53 have been allowed. By the foregoing, claims 54-64 have been added. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Applicants note for the benefit of the Examiner that the terms "first width vector" and "aligned vector" are used synonymously herein. Claim 1 as originally filed in this application recited at line 10 the term "first width vector." Applicants amended claim 1 in a Reply filed on January 24, 2001, to replace the term "first width vector" with the term "aligned vector." This amendment was made so that the same term used in other places of claim 1 (i.e., see the term "aligned vector" used in claim 1 at lines 2, 6 and 9) was also used in line 10. For purposes of clarity, however, Applicants note that the terms are used herein synonymously. Thus, the amendment is not intended to narrow the scope of claim 1.

This interpretation of the terms "first width vector" and "aligned vector" is fully supported by claim 1 as originally filed and by the specification. See, for example, page 10, lines 7-10, which states: "The alignment unit 312 receives two vectors from two source registers such as vs 306 and vt 308. Then, the alignment unit 312 extracts an aligned vector from the two vectors and stores it into a destination register such as vd 310." Note that the term "aligned vector" in this text from the specification has the same meaning as the term "first width vector" from original claim 1.

Favorable consideration of all pending claims is respectfully requested. The Examiner is invited to telephone the undersigned representative with any questions or comments or if he believes that an interview might be useful for any reason. Reconsideration of this application and entry of the above Amendments are respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

A handwritten signature in black ink, appearing to read "MBR", enclosed within a large, loopy circular flourish.

Michael B. Ray
Attorney for Applicants
Registration No. 33,997

Date: 5/22/02

1100 New York Avenue, N.W.
Suite 600
Washington, D.C. 20005-3934
(202) 371-2600

Version with markings to show changes made

In the Claims:

Please add new claims 54-64.

SKGF_DC1:5954.2

From: FedEx <donotreply@fedex.com>
To: <donf@skgf.com>
Date: 6/4/04 12:29PM
Subject: FedEx shipment 791857416715

Our records indicate that the shipment sent from Donald J. Featherstone/sterne kessler go to Timothy J. van Hook has been delivered.

The package was delivered on 06/04/2004 at 9:27 AM and signed for or released by .VANHOOK.

The ship date of the shipment was 06/03/2004.

The tracking number of this shipment was 791857416715.

FedEx appreciates your business. For more information about FedEx services, please visit our web site at <http://www.fedex.com>

To track the status of this shipment online please use the following:

http://www.fedex.com/cgi-bin/tracking?tracknumbers=791857416715&action=track&language=english&cntry_code=us

Disclaimer

FedEx has not validated the authenticity of any email address.



Robert Greene Sterne
Edward J. Kessler
Jorge A. Goldstein
David K.S. Cornwell
Robert W. Esmond
Tracy-Gene G. Durkin
Michele A. Cimbala
Michael B. Ray
Robert E. Sokohl
Eric K. Steffe
Michael Q. Lee
Steven R. Ludwig
John M. Covert
Linda E. Alcorn
Robert C. Millonig
Lawrence B. Bugaisky
Donald J. Featherstone
Michael V. Messinger

Judith U. Kim
Timothy J. Shea, Jr.
Patrick E. Garrett
Heidi L. Kraus
Edward W. Yee
Albert L. Ferro*
Donald R. Banowitz
Peter A. Jackman
Teresa U. Medler
Jeffrey S. Weaver
Kendrick P. Patterson
Vincent L. Capuano
Eldora Ellison Floyd
Thomas C. Fiala
Brian J. Del Buono
Virgil Lee Beaton
Kimberly N. Reddick
Theodore A. Wood

Elizabeth J. Haanes
Joseph S. Ostroff
Frank R. Cottingham
Christine M. Lhuffer
Rae Lynn Prengaman
Jane Shershenovich*
Lawrence J. Carroll*
George S. Bardmesser
Daniel A. Klein*
Jason D. Eisenberg
Michael D. Specht
Andrea J. Kamagie
Tracy L. Muller
LuAnne M. DeSantis
John J. Figueroa
Ann E. Summerfield
Tiera S. Coston*
Aric W. Ledford*

Michael D. Specht
Jessica L. Parezo
Timothy A. Doyle*
Cynthia M. Bouchez
Nicole D. Dretar*
Ted J. Ebersole

Registered Patent Agents*
Karen R. Markowicz
Nancy J. Leith
Helene C. Carlson
Gaby L. Longworth
Matthew J. Dowd
Aaron L. Schwartz
Mary B. Jung
Katrina Y. Pei Quach
Bryan L. Skelton
Robert A. Schwartzman

Teresa A. Colella
Jeffrey S. Lundgren
Victoria S. Rutherford
Eric D. Hayes
Michelle K. Holcubek
Robert H. DeSelms
Simon J. Elliott
Julie A. Heider
Mia Mukerjee
Scott M. Woodhouse

Of Counsel
Kenneth C. Bass III
Evan R. Smith
Marvin C. Guthrie
*Admitted only in Maryland
*Admitted only in Virginia
*Practice Limited to Federal Agencies

September 22, 2004

WRITER'S DIRECT NUMBER:
(202) 772-8629

INTERNET ADDRESS:
DONF@SKGF.COM

William A. Huffman
16205 Roseleaf Lane
Los Gatos, CA 95032-3610

Via Federal Express

Re: U.S. Patent Nos. 5,933,650 & 6,266,758; Issued: August 3, 1999 & July 24, 2001
U.S. Patent Application No. 09/662,832; Filed: September 15, 2000
For: **Alignment and Ordering of Vector Elements for Single Instruction
Multiple Data Processing**
Inventors: Van Hook *et al.*
Our Refs: 1778.0100000, 1778.0100001, and 1778.0100002

Dear Mr. Huffman:

Our law firm is handling a family of patents on which you were named as an inventor. This patent family specifically includes the following:

- U.S. Patent No. 5,933,650, issued August 3, 1999;
- U.S. Patent No. 6,266,758, issued July 24, 2001; and
- U.S. Patent Application No. 09/662,832, filed September 15, 2000.

Each of these documents is entitled "Alignment and Ordering of Vector Elements for Single Instruction Multiple Data (SIMD) Processing." All are based on the same patent specification. The initially filed patent application was owned by Silicon Graphics, Inc. However, the patent family is now owned by MIPS Technologies, Inc., our client.

When the initial patent application was filed, the law firm that handled the filing requested status under 37 C.F.R. § 1.47. However, the request did not adequately meet the requirements set forth in this Rule. Rule 1.47, if followed properly, can allow an application to be filed even though one or more of the inventors refuses to sign the Declaration or cannot be reached. Because the inadequate request for Rule 1.47 Status in the initial application was not discovered until recently, it has been carried through to the subsequently filed applications of this patent family.

William A. Huffman
September 22, 2004
Page 2

We recently brought this error to the attention of the U.S. Patent and Trademark Office (USPTO) and asked for direction in correcting it. In response, the USPTO has directed us to contact the inventors and ask each to sign new Declarations, one for each of the patent documents listed above.

Enclosed you will find the following documents:

1. The original patent application specification, as filed on October 9, 1997 (U.S. Patent Application No. 08/947,649), on which all three patent documents are based;
2. U.S. Patent No. 5,933,650, issued August 3, 1999 (from U.S. Patent Application No. 08/947,649, filed October 9, 1997), which includes an initial set of allowed claims;
3. U.S. Patent No. 6,266,758, issued July 24, 2001 (from U.S. Patent Application No. 09/263,798, filed March 5, 1999), which includes a second set of allowed claims;
4. A list of currently pending allowed claims for U.S. Patent Application No. 09/662,832;
5. A copy of the original, executed Declaration and Power of Attorney for Patent Application (in five parts) as originally filed in U.S. Patent Application No. 08/947,649 (now U.S. Patent No. 5,933,650);
6. A new Declaration for U.S. Patent No. 5,933,650;
7. A new Declaration for U.S. Patent No. 6,266,758;
8. A new Declaration for U.S. Patent Application No. 09/662,832; and
9. A copy of 37 C.F.R. § 10.18(b) and (c).

We ask that you please review these documents, with particular attention directed toward the allowed claims for each patent document.

A Declaration for a patent application is a document that: 1) confirms each inventor's residence, mailing address, and citizenship; 2) certifies that each inventor contributed to at least one claim of the claimed subject matter; 3) certifies that the specification and claims have been reviewed and are understood; and 4) certifies that each inventor acknowledges the duty to disclose information that is material to patentability.

William A. Huffman
September 22, 2004
Page 3

Please carefully review the three new Declaration documents and any information that we have entered onto them. Your "residence" address should be your city and state of residence, or, if you reside outside the United States, the city and country of residence. The "mailing" address is the (full) address at which you customarily receive mail. Either your home or business address is an acceptable mailing address. Please make any corrections, if necessary, **in blue ink** and then **initial and date in the margin**. Once the information on the Declarations is complete and correct, and after your review of the application and the allowed claims for each invention, please **sign and date** each Declaration **in blue ink** where indicated.

Every person who signs a document that is submitted to the USPTO makes a certification under 37 C.F.R. § 10.18(b) and (c). Therefore, a copy of this rule is also enclosed for your review.

For your convenience, we have provided a self-addressed, stamped return envelope for returning the signed Declarations to us. We ask that you attend to this matter as soon as possible.

Because U.S. Patent Application No. 09/662,832 has not yet issued as a patent, it is our obligation to remind you that a duty of disclosure continues throughout the entire patent application process and ends only with the actual issuance of a patent. Therefore, if you have or become aware of any information that might be considered material to patentability, please forward it to us immediately.

We, along with our client, greatly appreciate your assistance with this matter, and look forward to your return of the executed Declarations. In the meantime, if you have any comments or questions regarding this matter, please do not hesitate to contact us.

Very truly yours,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



Donald J. Featherstone

DJF/LMY:krd
Enclosures

312094_1.DOC

From: Origin ID: (202)371-2600
Donald J. Featherstone
Sierne Kessler Goldstein & Fox
1100 New York Avenue, NW

Washington, DC 20005



CL80426040504

SHIP TO: (408)356-8217

BILL SENDER

William A. Huffman

16205 Roseleaf Lane

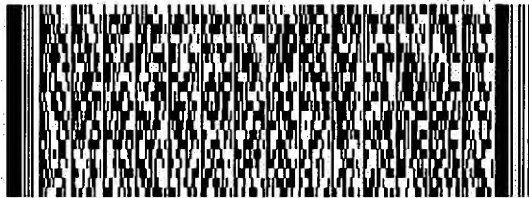
Los Gatos, CA 950323610

Ship Date: 22SEP04
Actual Wgt: 2 LB
System#: 1162221/INET1900
Account#: S *****

REF: 1778.0100002



Delivery Address Bar Code



STANDARD OVERNIGHT

THU

TRK# 7927 3610 3470

FORM
0201

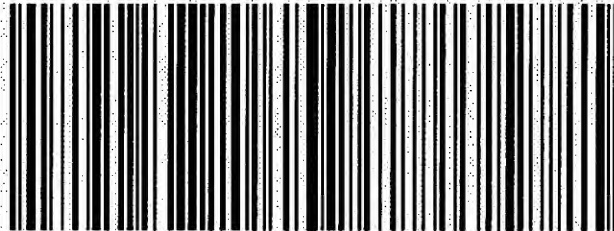
Deliver By:
23SEP04

SJC

AA

95032 -CA-US

NA SJCA



Shipping Label: Your shipment is complete

1. Use the 'Print' feature from your browser to send this page to your laser or inkjet printer.
2. Fold the printed page along the horizontal line.
3. Place label in shipping pouch and affix it to your shipment so that the barcode portion of the label can be read and scanned.

Warning: Use only the printed original label for shipping. Using a photocopy of this label for shipping purposes is fraudulent and could result in additional billing charges, along with the cancellation of your FedEx account number.

Use of this system constitutes your agreement to the service conditions in the current FedEx Service Guide, available on fedex.com. FedEx will not be responsible for any claim in excess of \$100 per package, whether the result of loss, damage, delay, non-delivery, misdelivery, or misinformation, unless you declare a higher value, pay an additional charge, document your actual loss and file a timely claim. Limitations found in the current FedEx Service Guide apply. Your right to recover from FedEx for any loss, including intrinsic value of the package, loss of sales, income interest, profit, attorney's fees, costs, and other forms of damage whether direct, incidental, consequential, or special is limited to the greater of \$100 or the authorized declared value. Recovery cannot exceed actual documented loss. Maximum for items of extraordinary value is \$500, e.g. jewelry, precious metals, negotiable instruments and other items listed in our Service Guide. Written claims must be filed within strict time limits, see current FedEx Service Guide.



Robert Greene Sterne
Edward J. Kessler
Jorge A. Goldstein
David K.S. Cornwell
Robert W. Esmond
Tracy-Gene G. Durkin
Michele A. Cimballa
Michael B. Ray
Robert E. Sokohl
Eric K. Steffe
Michael O. Lee
Steven R. Ludwig
John M. Covert
Linda E. Alcorn
Robert C. Millonig
Lawrence B. Bugalsky
Donald J. Featherstone
Michael V. Messinger

Judith U. Kim
Timothy J. Shea, Jr.
Patrick E. Garrett
Heidi L. Kraus
Edward W. Yee
Albert L. Ferro*
Donald R. Banowitz
Peter A. Jackman
Teresa U. Medler
Jeffrey S. Weaver
Kendrick P. Patterson
Vincent L. Capuano
Eldora Ellison Floyd
Thomas C. Fiala
Brian J. Del Buono
Virgil Lee Beaton
Kimberly N. Reddick
Theodore A. Wood

Elizabeth J. Haanes
Joseph S. Ostroff
Frank R. Cottingham
Christine M. Lhullier
Rae Lynn Prengaman
Jane Shershenovich*
Lawrence J. Carroll*
George S. Bardmesser
Daniel A. Klein*
Jason D. Eisenberg
Michael D. Specht
Andrea J. Kamage
Tracy L. Muller*
LuAnne M. DeSantis
John J. Figueroa
Ann E. Summerfield
Tiera S. Coston*
Aric W. Ledford*

Michael D. Specht
Jessica L. Parezo
Timothy A. Doyle*
Cynthia M. Bouchez
Nicole D. Dretar*
Ted J. Ebersole
Registered Patent Agents*
Karen R. Markowicz
Nancy J. Leith
Helene C. Carlson
Gaby L. Longsworth
Matthew J. Dowd
Aaron L. Schwartz
Mary B. Tung
Katrina Y. Pei Quach
Bryan L. Skelton
Robert A. Schwartzman

Teresa A. Cotella
Jeffrey S. Lundgren
Victoria S. Rutherford
Eric D. Hayes
Michelle K. Holoubek
Robert H. DeSels
Simon J. Elliott
Julie A. Heider
Mita Mukerjee
Scott M. Woodhouse
Of Counsel
Kenneth C. Bass III
Evan R. Smith
Marvin C. Guthrie
*Admitted only in Maryland
*Admitted only in Virginia
*Practice Limited to
Federal Agencies

September 22, 2004

WRITER'S DIRECT NUMBER:
(202) 772-8629

INTERNET ADDRESS:
DONF@SKGF.COM

Henry P. Moreton
140 Phillip Road
Woodside, CA 94062-2625

Via Federal Express

Re: U.S. Patent Nos. 5,933,650 & 6,266,758; Issued: August 3, 1999 & July 24, 2001
U.S. Patent Application No. 09/662,832; Filed: September 15, 2000

For: **Alignment and Ordering of Vector Elements for Single Instruction
Multiple Data Processing**

Inventors: Van Hook *et al.*

Our Refs: 1778.0100000, 1778.0100001, and 1778.0100002

Dear Mr. Moreton:

Our law firm is handling a family of patents on which you were named as an inventor. This patent family specifically includes the following:

- U.S. Patent No. 5,933,650, issued August 3, 1999;
- U.S. Patent No. 6,266,758, issued July 24, 2001; and
- U.S. Patent Application No. 09/662,832, filed September 15, 2000.

Each of these documents is entitled "Alignment and Ordering of Vector Elements for Single Instruction Multiple Data (SIMD) Processing." All are based on the same patent specification. The initially filed patent application was owned by Silicon Graphics, Inc. However, the patent family is now owned by MIPS Technologies, Inc., our client.

When the initial patent application was filed, the law firm that handled the filing requested status under 37 C.F.R. § 1.47. However, the request did not adequately meet the requirements set forth in this Rule. Rule 1.47, if followed properly, can allow an application to be filed even though one or more of the inventors refuses to sign the Declaration or cannot be reached. Because the inadequate request for Rule 1.47 Status in the initial application was not discovered until recently, it has been carried through to the subsequently filed applications of this patent family.

We recently brought this error to the attention of the U.S. Patent and Trademark Office (USPTO) and asked for direction in correcting it. In response, the USPTO has directed us to contact the inventors and ask each to sign new Declarations, one for each of the patent documents listed above.

Enclosed you will find the following documents:

1. The original patent application specification, as filed on October 9, 1997 (U.S. Patent Application No. 08/947,649), on which all three patent documents are based;
2. U.S. Patent No. 5,933,650, issued August 3, 1999 (from U.S. Patent Application No. 08/947,649, filed October 9, 1997), which includes an initial set of allowed claims;
3. U.S. Patent No. 6,266,758, issued July 24, 2001 (from U.S. Patent Application No. 09/263,798, filed March 5, 1999), which includes a second set of allowed claims;
4. A list of currently pending allowed claims for U.S. Patent Application No. 09/662,832;
5. A copy of the original, executed Declaration and Power of Attorney for Patent Application (in five parts) as originally filed in U.S. Patent Application No. 08/947,649 (now U.S. Patent No. 5,933,650);
6. A new Declaration for U.S. Patent No. 5,933,650;
7. A new Declaration for U.S. Patent No. 6,266,758;
8. A new Declaration for U.S. Patent Application No. 09/662,832; and
9. A copy of 37 C.F.R. § 10.18(b) and (c).

We ask that you please review these documents, with particular attention directed toward the allowed claims for each patent document.

A Declaration for a patent application is a document that: 1) confirms each inventor's residence, mailing address, and citizenship; 2) certifies that each inventor contributed to at least one claim of the claimed subject matter; 3) certifies that the specification and claims have been reviewed and are understood; and 4) certifies that each inventor acknowledges the duty to disclose information that is material to patentability.

Henry P. Moreton
September 22, 2004
Page 3

Please carefully review the three new Declaration documents and any information that we have entered onto them. Your "residence" address should be your city and state of residence, or, if you reside outside the United States, the city and country of residence. The "mailing" address is the (full) address at which you customarily receive mail. Either your home or business address is an acceptable mailing address. Please make any corrections, if necessary, **in blue ink** and then **initial and date in the margin**. Once the information on the Declarations is complete and correct, and after your review of the application and the allowed claims for each invention, please **sign and date** each Declaration **in blue ink** where indicated.

Every person who signs a document that is submitted to the USPTO makes a certification under 37 C.F.R. § 10.18(b) and (c). Therefore, a copy of this rule is also enclosed for your review.

For your convenience, we have provided a self-addressed, stamped return envelope for returning the signed Declarations to us. We ask that you attend to this matter as soon as possible.

Because U.S. Patent Application No. 09/662,832 has not yet issued as a patent, it is our obligation to remind you that a duty of disclosure continues throughout the entire patent application process and ends only with the actual issuance of a patent. Therefore, if you have or become aware of any information that might be considered material to patentability, please forward it to us immediately.

We, along with our client, greatly appreciate your assistance with this matter, and look forward to your return of the executed Declarations. In the meantime, if you have any comments or questions regarding this matter, please do not hesitate to contact us.

Very truly yours,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



Donald J. Featherstone

DJF/LMY:krd
Enclosures

312118_1.DOC

From: Origin ID: (202)371-2600
Donald J. Featherstone
Sterne Kessler Goldstein & Fox
1100 New York Avenue, NW

Washington, DC 20005



CLSD#26040504

SHIP TO: (202)772-8657

BILL SENDER

Henry P. Moreton

140 Phillip Road

Woodside, CA 940622625

Ship Date: 22SEP04
Actual Wgt: 3 LB
System#: 1162221/INET1900
Account#: S *****

REF: 1778.0100000



Delivery Address Bar Code

STANDARD OVERNIGHT

THU

Deliver By:
23SEP04

TRK# 7913 4448 9555

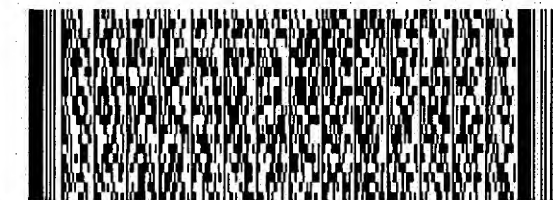
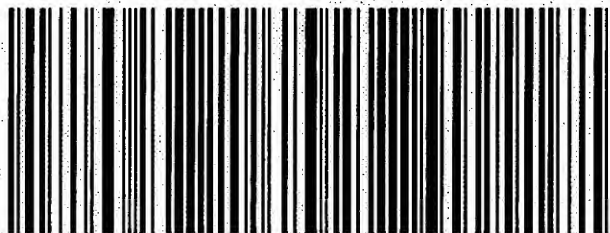
FORM
0201

SFO

AA

94062 -CA-US

XH PAOA



Shipping Label: Your shipment is complete

1. Use the 'Print' feature from your browser to send this page to your laser or inkjet printer.
2. Fold the printed page along the horizontal line.
3. Place label in shipping pouch and affix it to your shipment so that the barcode portion of the label can be read and scanned.

Warning: Use only the printed original label for shipping. Using a photocopy of this label for shipping purposes is fraudulent and could result in additional billing charges, along with the cancellation of your FedEx account number.

Use of this system constitutes your agreement to the service conditions in the current FedEx Service Guide, available on fedex.com. FedEx will not be responsible for any claim in excess of \$100 per package, whether the result of loss, damage, delay, non-delivery, misdelivery, or misinformation, unless you declare a higher value, pay an additional charge, document your actual loss and file a timely claim. Limitations found in the current FedEx Service Guide apply. Your right to recover from FedEx for any loss, including intrinsic value of the package, loss of sales, income interest, profit, attorney's fees, costs, and other forms of damage whether direct, incidental, consequential, or special is limited to the greater of \$100 or the authorized declared value. Recovery cannot exceed actual documented loss. Maximum for items of extraordinary value is \$500, e.g. jewelry, precious metals, negotiable instruments and other items listed in our Service Guide. Written claims must be filed within strict time limits, see current FedEx Service Guide.



Robert Greene Sterne
Edward J. Kessler
Jorge A. Goldstein
David K.S. Cornwell
Robert W. Esmond
Tracy-Gene G. Durkin
Michele A. Cimbalà
Michael B. Ray
Robert E. Sokohl
Eric K. Steffe
Michael Q. Lee
Steven R. Ludwig
John M. Covert
Linda E. Alcorn
Robert C. Millionig
Lawrence B. Bugalsky
Donald J. Featherstone
Michael V. Messinger

Judith U. Kim
Timothy J. Shea, Jr.
Patrick E. Garrett
Heidi L. Kraus
Edward W. Yee
Albert L. Ferro*
Donald R. Banowitz
Peter A. Jackman
Teresa U. Medler
Jeffrey S. Weaver
Kendrick P. Patterson
Vincent L. Capuano
Eldora Ellison Floyd
Thomas C. Fiala
Brian J. Del Buono
Virgil Lee Beaton
Kimberly N. Reddick
Theodore A. Wood

Elizabeth J. Haanes
Joseph S. Ostroff
Frank R. Cottingham
Christine M. Lhulier
Rae Lynn Prengaman
Jane Shershenovich*
Lawrence J. Carroll*
George S. Bardmesser
Daniel A. Klein*
Jason D. Eisenberg
Michael D. Specht
Andrea J. Kamage
Tracy L. Muller*
LuAnne M. DeSantis
John J. Figueroa
Ann E. Summerfield
Tiera S. Coston*
Aric W. Ledford*

Michael D. Specht
Jessica L. Parezo
Timothy A. Doyle*
Cynthia M. Bouchez
Nicole D. Dretar*
Ted J. Ebersole
Registered Patent Agents*
Karen R. Markowicz
Nancy J. Leith
Helene C. Carlson
Gaby L. Longworth
Matthew J. Dowd
Aaron L. Schwartz
Mary B. Tung
Katrina Y. Pei Quach
Bryan L. Skelton
Robert A. Schwartzman

Teresa A. Colella
Jeffrey S. Lundgren
Victoria S. Rutherford
Eric D. Hayes
Michelle K. Holoubek
Robert H. DeSelms
Simon J. Elliott
Julie A. Heider
Mita Mukerjee
Scott M. Woodhouse
Of Counsel
Kenneth C. Bass III
Evan R. Smith
Marvin C. Guthrie
*Admitted only in Maryland
*Admitted only in Virginia
*Practice Limited to Federal Agencies

September 22, 2004

WRITER'S DIRECT NUMBER:
(202) 772-8629
INTERNET ADDRESS:
DONF@SKGF.COM

Timothy J. Van Hook
224 Oakgrove Avenue
Atherton, CA 94027

Via Federal Express

Re: U.S. Patent Nos. 5,933,650 & 6,266,758; Issued: August 3, 1999 & July 24, 2001
U.S. Patent Application No. 09/662,832; Filed: September 15, 2000
For: **Alignment and Ordering of Vector Elements for Single Instruction
Multiple Data Processing**
Inventors: Van Hook *et al.*
Our Refs: 1778.0100000, 1778.0100001, and 1778.0100002

Dear Mr. Van Hook:

Our law firm is handling a family of patents on which you were named as an inventor. This patent family specifically includes the following:

- U.S. Patent No. 5,933,650, issued August 3, 1999;
- U.S. Patent No. 6,266,758, issued July 24, 2001; and
- U.S. Patent Application No. 09/662,832, filed September 15, 2000.

Each of these documents is entitled "Alignment and Ordering of Vector Elements for Single Instruction Multiple Data (SIMD) Processing." All are based on the same patent specification. The initially filed patent application was owned by Silicon Graphics, Inc. However, the patent family is now owned by MIPS Technologies, Inc., our client.

When the initial patent application was filed, the law firm that handled the filing requested status under 37 C.F.R. § 1.47. However, the request did not adequately meet the requirements set forth in this Rule. Rule 1.47, if followed properly, can allow an application to be filed even though one or more of the inventors refuses to sign the Declaration or cannot be reached. Because the inadequate request for Rule 1.47 Status in the initial application was not discovered until recently, it has been carried through to the subsequently filed applications of this patent family.

Timothy J. Van Hook
September 22, 2004
Page 2

We recently brought this error to the attention of the U.S. Patent and Trademark Office (USPTO) and asked for direction in correcting it. In response, the USPTO has directed us to contact the inventors and ask each to sign new Declarations, one for each of the patent documents listed above.

Enclosed you will find the following documents:

1. The original patent application specification, as filed on October 9, 1997 (U.S. Patent Application No. 08/947,649), on which all three patent documents are based;
2. U.S. Patent No. 5,933,650, issued August 3, 1999 (from U.S. Patent Application No. 08/947,649, filed October 9, 1997), which includes an initial set of allowed claims;
3. U.S. Patent No. 6,266,758, issued July 24, 2001 (from U.S. Patent Application No. 09/263,798, filed March 5, 1999), which includes a second set of allowed claims;
4. A list of currently pending allowed claims for U.S. Patent Application No. 09/662,832;
5. A copy of the original, executed Declaration and Power of Attorney for Patent Application (in five parts) as originally filed in U.S. Patent Application No. 08/947,649 (now U.S. Patent No. 5,933,650);
6. A new Declaration for U.S. Patent No. 5,933,650;
7. A new Declaration for U.S. Patent No. 6,266,758;
8. A new Declaration for U.S. Patent Application No. 09/662,832; and
9. A copy of 37 C.F.R. § 10.18(b) and (c).

We ask that you please review these documents, with particular attention directed toward the allowed claims for each patent document.

A Declaration for a patent application is a document that: 1) confirms each inventor's residence, mailing address, and citizenship; 2) certifies that each inventor contributed to at least one claim of the claimed subject matter; 3) certifies that the specification and claims have been reviewed and are understood; and 4) certifies that each inventor acknowledges the duty to disclose information that is material to patentability.

Timothy J. Van Hook
September 22, 2004
Page 3

Please carefully review the three new Declaration documents and any information that we have entered onto them. Your "residence" address should be your city and state of residence, or, if you reside outside the United States, the city and country of residence. The "mailing" address is the (full) address at which you customarily receive mail. Either your home or business address is an acceptable mailing address. Please make any corrections, if necessary, **in blue ink** and then **initial and date in the margin**. Once the information on the Declarations is complete and correct, and after your review of the application and the allowed claims for each invention, please **sign and date** each Declaration **in blue ink** where indicated.

Every person who signs a document that is submitted to the USPTO makes a certification under 37 C.F.R. § 10.18(b) and (c). Therefore, a copy of this rule is also enclosed for your review.

For your convenience, we have provided a self-addressed, stamped return envelope for returning the signed Declarations to us. We ask that you attend to this matter as soon as possible.

Because U.S. Patent Application No. 09/662,832 has not yet issued as a patent, it is our obligation to remind you that a duty of disclosure continues throughout the entire patent application process and ends only with the actual issuance of a patent. Therefore, if you have or become aware of any information that might be considered material to patentability, please forward it to us immediately.

We, along with our client, greatly appreciate your assistance with this matter, and look forward to your return of the executed Declarations. In the meantime, if you have any comments or questions regarding this matter, please do not hesitate to contact us.

Very truly yours,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



Donald J. Featherstone

DJF/LMY:krd
Enclosures

312080_1.DOC

From: Origin ID: (202)371-2600
Donald J. Feathersone
Sterne Kessler Goldstein & Fox
1100 New York Avenue, NW

Washington, DC 20005



CLS0#28040504

SHIP TO: (650)325-7605
Timothy J. Van Hook

BILL SENDER

224 Oakgrove Avenue

Atherton, CA 94027

Ship Date: 22SEP04
Actual Wgt: 2 LB
System#: 1162221/NET1900
Account#: S *****

REF: 1778.0100000



Delivery Address Bar Code

STANDARD OVERNIGHT

THU

Deliver By:
23SEP04

TRK# **7913 4357 9263**

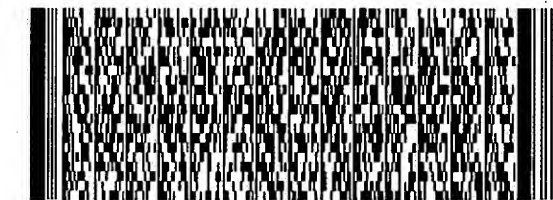
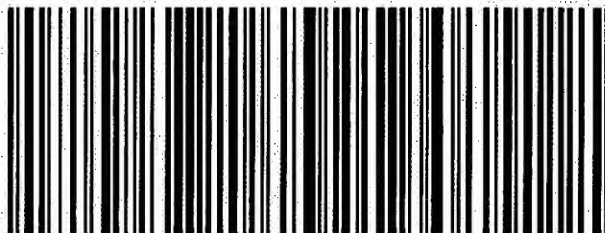
FORM
0201

SFO

A2

94027 -CA-US

XH HGTA



Shipping Label: Your shipment is complete

1. Use the 'Print' feature from your browser to send this page to your laser or inkjet printer.
2. Fold the printed page along the horizontal line.
3. Place label in shipping pouch and affix it to your shipment so that the barcode portion of the label can be read and scanned.

Warning: Use only the printed original label for shipping. Using a photocopy of this label for shipping purposes is fraudulent and could result in additional billing charges, along with the cancellation of your FedEx account number.

Use of this system constitutes your agreement to the service conditions in the current FedEx Service Guide, available on fedex.com. FedEx will not be responsible for any claim in excess of \$100 per package, whether the result of loss, damage, delay, non-delivery, misdelivery, or misinformation, unless you declare a higher value, pay an additional charge, document your actual loss and file a timely claim. Limitations found in the current FedEx Service Guide apply. Your right to recover from FedEx for any loss, including intrinsic value of the package, loss of sales, income interest, profit, attorney's fees, costs, and other forms of damage whether direct, incidental, consequential, or special is limited to the greater of \$100 or the authorized declared value. Recovery cannot exceed actual documented loss. Maximum for items of extraordinary value is \$500, e.g. jewelry, precious metals, negotiable instruments and other items listed in our Service Guide. Written claims must be filed within strict time limits, see current FedEx Service Guide.



Robert Greene Sterne
Edward J. Kessler
Jorge A. Goldstein
David K.S. Cornwell
Robert W. Esmond
Tracy-Gene G. Durkin
Michele A. Cimbala
Michael B. Ray
Robert E. Sokohl
Eric K. Steffe
Michael Q. Lee
Steven R. Ludwig
John M. Covert
Linda E. Alcorn
Robert C. Millonig
Lawrence B. Bugalsky
Donald J. Featherstone
Michael V. Messinger

Judith U. Kim
Timothy J. Shea, Jr.
Patrick E. Garrett
Heidi L. Kraus
Edward W. Yee
Albert L. Ferro
Donald R. Banowitz
Peter A. Jackman
Teresa U. Medler
Jeffrey S. Weaver
Kendrick P. Patterson
Vincent L. Capuano
Eldora Ellison Floyd
Thomas C. Fiala
Brian J. Del Buono
Virgil Lee Beaton
Kimberly N. Reddick
Theodore A. Wood

Elizabeth J. Haanes
Joseph S. Ostroff
Frank R. Cottingham
Christine M. Thullier
Rae Lynn Prengaman
Jane Shershenovich
Lawrence J. Carroll
George S. Bardmesser
Daniel A. Klein
Jason D. Eisenberg
Michael D. Specht
Andrea J. Kamage
Tracy L. Muller
LuAnne M. DeSantis
John J. Figueroa
Ann E. Summerfield
Tiera S. Coston
Aric W. Ledford

Michael D. Specht
Jessica L. Parezo
Timothy A. Doyle
Cynthia M. Bouchez
Nicole D. Dretar
Ted J. Ebersole
Registered Patent Agents*
Karen R. Markowicz
Nancy J. Leith
Helene C. Carlson
Gaby L. Longworth
Matthew J. Dowd
Aaron L. Schwartz
Mary B. Tung
Katrina Y. Pei Quach
Bryan L. Skelton
Robert A. Schwartzman

Teresa A. Colella
Jeffrey S. Lundgren
Victoria S. Rutherford
Eric D. Hayes
Michelle K. Holcubek
Robert H. DeSelms
Simon J. Elliott
Julie A. Heider
Mita Mukerjee
Scott M. Woodhouse
Of Counsel
Kenneth C. Bass III
Evan R. Smith
Marvin C. Guthrie
*Admitted only in Maryland
*Admitted only in Virginia
*Practice Limited to Federal Agencies

September 22, 2004

WRITER'S DIRECT NUMBER:
(202) 772-8629
INTERNET ADDRESS:
DONF@SKGF.COM

Earl A. Killian
27961 Central Drive
Los Altos Hills, CA 94022

Via Federal Express

Re: U.S. Patent Nos. 5,933,650 & 6,266,758; Issued: August 3, 1999 & July 24, 2001
U.S. Patent Application No. 09/662,832; Filed: September 15, 2000
For: **Alignment and Ordering of Vector Elements for Single Instruction
Multiple Data Processing**
Inventors: Van Hook *et al.*
Our Refs: 1778.0100000, 1778.0100001, and 1778.0100002

Dear Mr. Killian:

Our law firm is handling a family of patents on which you were named as an inventor. This patent family specifically includes the following:

- U.S. Patent No. 5,933,650, issued August 3, 1999;
- U.S. Patent No. 6,266,758, issued July 24, 2001; and
- U.S. Patent Application No. 09/662,832, filed September 15, 2000.

Each of these documents is entitled "Alignment and Ordering of Vector Elements for Single Instruction Multiple Data (SIMD) Processing." All are based on the same patent specification. The initially filed patent application was owned by Silicon Graphics, Inc. However, the patent family is now owned by MIPS Technologies, Inc., our client.

When the initial patent application was filed, the law firm that handled the filing requested status under 37 C.F.R. § 1.47. However, the request did not adequately meet the requirements set forth in this Rule. Rule 1.47, if followed properly, can allow an application to be filed even though one or more of the inventors refuses to sign the Declaration or cannot be reached. Because the inadequate request for Rule 1.47 Status in the initial application was not discovered until recently, it has been carried through to the subsequently filed applications of this patent family.

Earl A. Killian
September 22, 2004
Page 2

We recently brought this error to the attention of the U.S. Patent and Trademark Office (USPTO) and asked for direction in correcting it. In response, the USPTO has directed us to contact the inventors and ask each to sign new Declarations, one for each of the patent documents listed above.

Enclosed you will find the following documents:

1. The original patent application specification, as filed on October 9, 1997 (U.S. Patent Application No. 08/947,649), on which all three patent documents are based;
2. U.S. Patent No. 5,933,650, issued August 3, 1999 (from U.S. Patent Application No. 08/947,649, filed October 9, 1997), which includes an initial set of allowed claims;
3. U.S. Patent No. 6,266,758, issued July 24, 2001 (from U.S. Patent Application No. 09/263,798, filed March 5, 1999), which includes a second set of allowed claims;
4. A list of currently pending allowed claims for U.S. Patent Application No. 09/662,832;
5. A copy of the original, executed Declaration and Power of Attorney for Patent Application (in five parts) as originally filed in U.S. Patent Application No. 08/947,649 (now U.S. Patent No. 5,933,650);
6. A new Declaration for U.S. Patent No. 5,933,650;
7. A new Declaration for U.S. Patent No. 6,266,758;
8. A new Declaration for U.S. Patent Application No. 09/662,832; and
9. A copy of 37 C.F.R. § 10.18(b) and (c).

We ask that you please review these documents, with particular attention directed toward the allowed claims for each patent document.

A Declaration for a patent application is a document that: 1) confirms each inventor's residence, mailing address, and citizenship; 2) certifies that each inventor contributed to at least one claim of the claimed subject matter; 3) certifies that the specification and claims have been reviewed and are understood; and 4) certifies that each inventor acknowledges the duty to disclose information that is material to patentability.

Earl A. Killian
September 22, 2004
Page 3

Please carefully review the three new Declaration documents and any information that we have entered onto them. Your "residence" address should be your city and state of residence, or, if you reside outside the United States, the city and country of residence. The "mailing" address is the (full) address at which you customarily receive mail. Either your home or business address is an acceptable mailing address. Please make any corrections, if necessary, **in blue ink** and then **initial and date in the margin**. Once the information on the Declarations is complete and correct, and after your review of the application and the allowed claims for each invention, please **sign and date** each Declaration **in blue ink** where indicated.

Every person who signs a document that is submitted to the USPTO makes a certification under 37 C.F.R. § 10.18(b) and (c). Therefore, a copy of this rule is also enclosed for your review.

For your convenience, we have provided a self-addressed, stamped return envelope for returning the signed Declarations to us. We ask that you attend to this matter as soon as possible.

Because U.S. Patent Application No. 09/662,832 has not yet issued as a patent, it is our obligation to remind you that a duty of disclosure continues throughout the entire patent application process and ends only with the actual issuance of a patent. Therefore, if you have or become aware of any information that might be considered material to patentability, please forward it to us immediately.

We, along with our client, greatly appreciate your assistance with this matter, and look forward to your return of the executed Declarations. In the meantime, if you have any comments or questions regarding this matter, please do not hesitate to contact us.

Very truly yours,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



Donald J. Featherstone

DJF/LMY:krd
Enclosures

312159_1.DOC

From: Origin ID: (202)371-2600
Donald J. Featherstone
Steme Kessler Goldstein & Fox
1100 New York Avenue, NW

Washington, DC 20005



CL50126040504

SHIP TO: (650)949-3339

BILL SENDER

Earl A. Killian

27961 Central Drive

Los Altos Hills, CA 94022

Ship Date: 22SEP04
Actual Wgt: 2 LB
System#: 1162221/INET1900
Account#: S *****

REF: 1778.0100001.



Delivery Address Bar Code

STANDARD OVERNIGHT

THU

Deliver By:
23SEP04

TRK# 7919 3817 5275

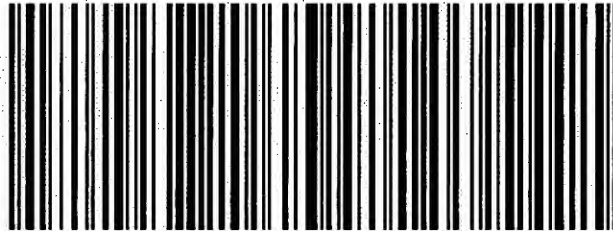
FORM
0201

SJC

AA

94022 -CA-US

NA NUQA



Shipping Label: Your shipment is complete

1. Use the 'Print' feature from your browser to send this page to your laser or inkjet printer.
2. Fold the printed page along the horizontal line.
3. Place label in shipping pouch and affix it to your shipment so that the barcode portion of the label can be read and scanned.

Warning: Use only the printed original label for shipping. Using a photocopy of this label for shipping purposes is fraudulent and could result in additional billing charges, along with the cancellation of your FedEx account number.

Use of this system constitutes your agreement to the service conditions in the current FedEx Service Guide, available on fedex.com. FedEx will not be responsible for any claim in excess of \$100 per package, whether the result of loss, damage, delay, non-delivery, misdelivery, or misinformation, unless you declare a higher value, pay an additional charge, document your actual loss and file a timely claim. Limitations found in the current FedEx Service Guide apply. Your right to recover from FedEx for any loss, including intrinsic value of the package, loss of sales, income interest, profit, attorney's fees, costs, and other forms of damage whether direct, incidental, consequential, or special is limited to the greater of \$100 or the authorized declared value. Recovery cannot exceed actual documented loss. Maximum for items of extraordinary value is \$500, e.g. jewelry, precious metals, negotiable instruments and other items listed in our Service Guide. Written claims must be filed within strict time limits, see current FedEx Service Guide.



Robert Greene Sterne
Edward J. Kessler
Jorge A. Goldstein
David K.S. Cornwell
Robert W. Esmond
Tracy-Gene G. Durkin
Michele A. Cimbala
Michael B. Ray
Robert E. Sokohl
Eric K. Steffe
Michael Q. Lee
Steven R. Ludwig
John M. Covert
Linda E. Alcorn
Robert C. Millonig
Lawrence B. Bugalsky
Donald J. Featherstone
Michael V. Messinger

Judith U. Kim
Timothy J. Shea, Jr.
Patrick E. Garrett
Heidi L. Kraus
Edward W. Yee
Albert L. Ferro*
Donald R. Banowitz
Peter A. Jackman
Teresa U. Medler
Jeffrey S. Weaver
Kendrick P. Patterson
Vincent L. Capuano
Eldora Ellison Floyd
Thomas C. Fiala
Brian J. Del Buono
Virgil Lee Beason
Kimberly N. Reddick
Theodore A. Wood

Elizabeth J. Haanes
Joseph S. Ostroff
Frank R. Cottingham
Christine M. Lhulier
Rae Lynn Prengaman
Jane Shershenovich*
Lawrence J. Carroll*
George S. Bardmesser
Daniel A. Klein*
Jason D. Eisenberg
Michael D. Specht
Andrea J. Kamage
Tracy L. Muller
LuAnne M. DeSantis
John J. Figueroa
Ann E. Summerfield
Tiera S. Coston*
Aric W. Ledford*

Michael D. Specht
Jessica L. Parezo
Timothy A. Doyle*
Cynthia M. Bouchez
Nicole D. Dretar*
Ted J. Ebersole

Registered Patent Agents*

Karen R. Markowicz
Nancy J. Leith
Helene C. Carlson
Gaby L. Longworth
Matthew J. Dowd
Aaron L. Schwartz
Mary B. Jung
Katrina Y. Pei Quach
Bryan L. Skelton
Robert A. Schwartzman

Teresa A. Colella
Jeffrey S. Lundgren
Victoria S. Rutherford
Eric D. Hayes
Michelle K. Holoubek
Robert H. DeSelms
Simon J. Elliott
Julie A. Heider
Mita Mukerjee
Scott M. Woodhouse

Of Counsel

Kenneth C. Bass III
Evan R. Smith
Marvin C. Guthrie
*Admitted only in Maryland
*Admitted only in Virginia
*Practice Limited to Federal Agencies

September 22, 2004

WRITER'S DIRECT NUMBER:
(202) 772-8629

INTERNET ADDRESS:
DONF@SKGF.COM

Peter Yan-Tek Hsu
1 Rausch Street, Unit F
San Francisco, CA 94103

Via Federal Express

Re: U.S. Patent Nos. 5,933,650 & 6,266,758; Issued: August 3, 1999 & July 24, 2001
U.S. Patent Application No. 09/662,832; Filed: September 15, 2000
For: **Alignment and Ordering of Vector Elements for Single Instruction
Multiple Data Processing**
Inventors: Van Hook *et al.*
Our Refs: 1778.0100000, 1778.0100001, and 1778.0100002

Dear Mr. Hsu:

Our law firm is handling a family of patents on which you were named as an inventor. This patent family specifically includes the following:

- U.S. Patent No. 5,933,650, issued August 3, 1999;
- U.S. Patent No. 6,266,758, issued July 24, 2001; and
- U.S. Patent Application No. 09/662,832, filed September 15, 2000.

Each of these documents is entitled "Alignment and Ordering of Vector Elements for Single Instruction Multiple Data (SIMD) Processing." All are based on the same patent specification. The initially filed patent application was owned by Silicon Graphics, Inc. However, the patent family is now owned by MIPS Technologies, Inc., our client.

When the initial patent application was filed, the law firm that handled the filing requested status under 37 C.F.R. § 1.47. However, the request did not adequately meet the requirements set forth in this Rule. Rule 1.47, if followed properly, can allow an application to be filed even though one or more of the inventors refuses to sign the Declaration or cannot be reached. Because the inadequate request for Rule 1.47 Status in the initial application was not discovered until recently, it has been carried through to the subsequently filed applications of this patent family.

Peter Yan-Tek Hsu
September 22, 2004
Page 2

We recently brought this error to the attention of the U.S. Patent and Trademark Office (USPTO) and asked for direction in correcting it. In response, the USPTO has directed us to contact the inventors and ask each to sign new Declarations, one for each of the patent documents listed above.

Enclosed you will find the following documents:

1. The original patent application specification, as filed on October 9, 1997 (U.S. Patent Application No. 08/947,649), on which all three patent documents are based;
2. U.S. Patent No. 5,933,650, issued August 3, 1999 (from U.S. Patent Application No. 08/947,649, filed October 9, 1997), which includes an initial set of allowed claims;
3. U.S. Patent No. 6,266,758, issued July 24, 2001 (from U.S. Patent Application No. 09/263,798, filed March 5, 1999), which includes a second set of allowed claims;
4. A list of currently pending allowed claims for U.S. Patent Application No. 09/662,832;
5. A copy of the original, executed Declaration and Power of Attorney for Patent Application (in five parts) as originally filed in U.S. Patent Application No. 08/947,649 (now U.S. Patent No. 5,933,650);
6. A new Declaration for U.S. Patent No. 5,933,650;
7. A new Declaration for U.S. Patent No. 6,266,758;
8. A new Declaration for U.S. Patent Application No. 09/662,832; and
9. A copy of 37 C.F.R. § 10.18(b) and (c).

We ask that you please review these documents, with particular attention directed toward the allowed claims for each patent document.

A Declaration for a patent application is a document that: 1) confirms each inventor's residence, mailing address, and citizenship; 2) certifies that each inventor contributed to at least one claim of the claimed subject matter; 3) certifies that the specification and claims have been reviewed and are understood; and 4) certifies that each inventor acknowledges the duty to disclose information that is material to patentability.

Peter Yan-Tek Hsu
September 22, 2004
Page 3

Please carefully review the three new Declaration documents and any information that we have entered onto them. Your "residence" address should be your city and state of residence, or, if you reside outside the United States, the city and country of residence. The "mailing" address is the (full) address at which you customarily receive mail. Either your home or business address is an acceptable mailing address. Please make any corrections, if necessary, **in blue ink** and then **initial and date in the margin**. Once the information on the Declarations is complete and correct, and after your review of the application and the allowed claims for each invention, please **sign and date** each Declaration **in blue ink** where indicated.

Every person who signs a document that is submitted to the USPTO makes a certification under 37 C.F.R. § 10.18(b) and (c). Therefore, a copy of this rule is also enclosed for your review.

For your convenience, we have provided a self-addressed, stamped return envelope for returning the signed Declarations to us. We ask that you attend to this matter as soon as possible.

Because U.S. Patent Application No. 09/662,832 has not yet issued as a patent, it is our obligation to remind you that a duty of disclosure continues throughout the entire patent application process and ends only with the actual issuance of a patent. Therefore, if you have or become aware of any information that might be considered material to patentability, please forward it to us immediately.

We, along with our client, greatly appreciate your assistance with this matter, and look forward to your return of the executed Declarations. In the meantime, if you have any comments or questions regarding this matter, please do not hesitate to contact us.

Very truly yours,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



Donald J. Featherstone

DJF/LMY:krd
Enclosures

312082_1.DOC

From: Origin ID: (202)371-2600
Donald J. Featherstone
Sterne Kessler Goldstein & Fox
1100 New York Avenue, NW

Washington, DC 20005



CLS0126040504

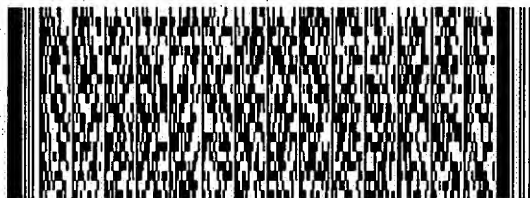
SHIP TO: (415)819-4096

BILL SENDER

Peter Yan-Tek Hsu

1 Rausch Street, Unit F

San Francisco, CA 94103



Ship Date: 22SEP04
Actual Wgt: 2 LB
System#: 1162221/INET1900
Account#: S *****

REF: 1778.0100001



Delivery Address Bar Code

STANDARD OVERNIGHT

THU

TRK# 7920 9505 7606

FORM
0201

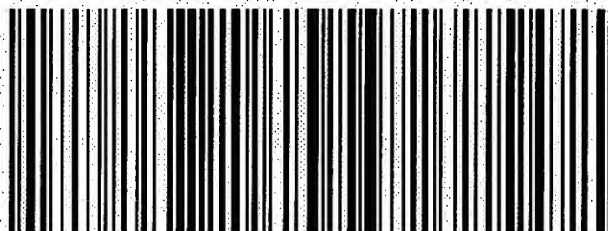
Deliver By:
23SEP04

SFO

A1

94103 -CA-US

XH NDBA



Shipping Label: Your shipment is complete

1. Use the 'Print' feature from your browser to send this page to your laser or inkjet printer.
2. Fold the printed page along the horizontal line.
3. Place label in shipping pouch and affix it to your shipment so that the barcode portion of the label can be read and scanned.

Warning: Use only the printed original label for shipping. Using a photocopy of this label for shipping purposes is fraudulent and could result in additional billing charges, along with the cancellation of your FedEx account number.

Use of this system constitutes your agreement to the service conditions in the current FedEx Service Guide, available on fedex.com. FedEx will not be responsible for any claim in excess of \$100 per package, whether the result of loss, damage, delay, non-delivery, misdelivery, or misinformation, unless you declare a higher value, pay an additional charge, document your actual loss and file a timely claim. Limitations found in the current FedEx Service Guide apply. Your right to recover from FedEx for any loss, including intrinsic value of the package, loss of sales, income interest, profit, attorney's fees, costs, and other forms of damage whether direct, incidental, consequential, or special is limited to the greater of \$100 or the authorized declared value. Recovery cannot exceed actual documented loss. Maximum for items of extraordinary value is \$500, e.g. jewelry, precious metals, negotiable instruments and other items listed in our Service Guide. Written claims must be filed within strict time limits, see current FedEx Service Guide.

UNITED STATES PATENT APPLICATION

FOR

ALIGNMENT AND ORDERING OF VECTOR ELEMENTS FOR SINGLE
INSTRUCTION MULTIPLE DATA PROCESSING

Inventors:

Timothy J. van Hook

Peter Hsu

William Huffman

Henry P. Moreton

Earl Killian

Prepared by:

WAGNER, MURABITO & HAO

Two North Market Street

Third Floor

San Jose, California 95113

ALIGNMENT AND ORDERING OF VECTOR ELEMENTS FOR SINGLE INSTRUCTION MULTIPLE DATA PROCESSING

FIELD OF THE INVENTION

5 The present invention relates to the field of single instruction multiple data vector (SIMD) processing. More particularly, the present claimed invention relates to alignment and ordering vector elements for SIMD processing.

10 BACKGROUND ART

 Today, most processors in microcomputer systems provide a 64-bit wide datapath architecture. The 64-bit datapath allows operations such as read, write, add, subtract, and multiply on the entire 64 bits of data at once. However, for many applications the types of data involved simply do not
15 require the full 64 bits. In media signal processing (MDMX) applications, for example, the light and sound values are usually represented in 8, 12, 16, or 24 bit numbers. This is because people typically are not able to distinguish the levels of light and sound beyond the levels represented by these numbers of bits. Hence, data types in MDMX applications typically require less than the
20 full 64 bits provided in the datapath in most computer systems.

 To efficiently utilize the entire datapath, the current generation of processors typically utilizes a single instruction multiple data (SIMD) method. According to this method, a multitude of smaller numbers are packed into
25 the 64 bit doubleword as elements, each of which is then operated on independently and in parallel. Prior Art Figure 1 illustrates an exemplary single instruction multiple data (SIMD) method. Registers, vs and vt, in a

processor are of 64-bit width. Each register is packed with four 16-bit data elements fetched from memory: register vs contains vs[0], vs[1], vs[2], and vs[3] and register vt contains vt[0], vt[1], vt[2], and vt[3]. The registers in essence contain a vector of N elements. To add elements of matching index, an add instruction adds, independently, each of the element pairs of matching index from vs and vt. A third register, vd, of 64-bit width may be used to store the result. For example, vs[0] is added to vt[0] and its result is stored into vd[0]. Similarly, vd[1], vd[2], and vd[3] store the sum of vs and vt elements of corresponding indexes. Hence, a single add operation on the 64-bit vector results in 4 simultaneous additions on each of the 16-bit elements. On the other hand, if 8-bit elements were packed into the registers, one add operation performs 8 independent additions in parallel. Consequently, when a SIMD arithmetic instruction such as addition, subtraction, or multiply, is performed on the data in the 64-bit datapath, the operation actually performs multiple numbers of operations independently and in parallel on each of the smaller elements comprising the 64 bit datapath. In SIMD vector operation, processors typically require alignment to the data type size of 64-bit doubleword on a load. This alignment ensures that the SIMD vector operations occur on aligned boundaries of a 64-bit doubleword boundary.

20

Unfortunately, the elements within application data vectors are frequently not 64-bit doubleword aligned for SIMD operations. For example, data elements stored in a memory unit are loaded into registers in a chunk such as a 64-bit doubleword format. To operate on the individual elements, the elements are loaded into a register. The order of the elements in the register remain the same as the order in the original memory. Accordingly, the elements may not be properly aligned for a SIMD operation.

Traditionally, when elements are not aligned with a proper boundary as required for a SIMD vector operation, the non-aligned vector processing have typically been reduced to scalar processing. That is, operations took
5 place one element at a time instead of simultaneous multiple operations. Consequently, SIMD vector operations lost parallelism and performance advantages when the vector elements were not properly aligned.

Furthermore, many media applications require a specific ordering for
10 the elements within a SIMD vector. Since elements necessary for SIMD processing are commonly stored in multiple 64-bit doublewords with other elements, these elements need to be selected and assembled into a vector of desired order. For example, multiple channel data are commonly stored in separate arrays or interleaved in a single array. Processing the data requires
15 interleaving or deinterleaving the multiple channels. Other applications require SIMD vector operations on transposed 2 dimensional arrays of data. Yet other applications reverse the order of elements in an array as in FFTs, DCTs, and convolution algorithms.

20 Thus, what is needed is a method for aligning and ordering elements for more efficient SIMD vector operations by providing computational parallelism.

SUMMARY OF THE INVENTION

The present invention provides alignment and ordering of vector elements for SIMD processing. The present invention is implemented in a computer system including a processor having a plurality of registers. In the alignment of vector elements for SIMD processing, one vector is loaded from a memory unit into a first register and another vector is loaded from the memory unit into a second register. The first vector contains a first byte of an aligned vector to be generated. Then, a starting byte specifying the first byte of an aligned vector is determined. Next, a vector is extracted from the first register and the second register beginning from the first bit in the first byte of the first register continuing through the bits in the second register. Finally, the extracted vector is replicated into a third register such that the third register contains a plurality of elements aligned for SIMD processing. In the ordering of vector elements for SIMD processing, a first vector is loaded from a memory unit into a first register and a second vector is loaded from the memory unit into a second register. Then, a subset of elements is selected from the first register and the second register. The elements from the subset are then replicated into the elements in the third register in a particular order suitable for subsequent SIMD vector processing.

20

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention:

5

Prior Art Figure 1 illustrates an exemplary single instruction multiple data (SIMD) instruction method.

Figure 2 illustrates a block diagram of an exemplary computer system for implementing the present invention.

10 Figure 3 illustrates a block diagram of an exemplary datapath for aligning and ordering vector elements.

Figure 4 illustrates a block diagram of an alignment unit in a processor for aligning a vector of elements.

15 Figure 5 illustrates a flow diagram of the steps involved in extracting an aligned vector from two exemplary vectors.

Figure 6A illustrates a block diagram of a full byte-mode crossbar circuit used in generating a vector of elements from elements of two vector registers.

Figure 6B shows a more detailed diagram of the operation of an exemplary AND gate associated with element 7 in the first register, vs.

20 Figure 7 illustrates shuffle operations for ordering 8-bit elements in a 64-bit doubleword.

Figure 8A illustrates a block diagram of a shuffle operation, which converts four unsigned upper bytes (i.e., 8 bits) in a source register to four 16-bit halves in a destination register.

25 Figure 8B illustrates a block diagram of a shuffle operation, which converts a vector of unsigned low 4 bytes from a source register to four 16-bit halves in a destination register.

Figure 8C illustrates a block diagram of a shuffle operation, which converts a vector of signed upper 4 bytes from a source register to four 16-bit halves in a destination register by replicating the signs across the upper bytes in the halves.

5 Figure 8D illustrates a block diagram of a shuffle operation, which converts a vector of signed low 4 bytes from a source register to four 16-bit halves in a destination register by replicating the signs across the upper bytes in the halves.

Figure 8E illustrates a block diagram of a shuffle operation, which
10 replicates the odd elements of 8 8-bit elements from each of two source registers into 8 elements in a destination vector register.

Figure 8F illustrates a block diagram of a shuffle operation, which replicates the even elements of 8 8-bit elements from each of two source registers into 8 elements in a destination vector register.

15 Figure 8G illustrates a block diagram of a shuffle operation, which replicates the upper 4 elements of 8 8-bit elements from each of two source registers into 8 elements in a destination vector register.

Figure 8H illustrates a block diagram of a shuffle operation, which replicates the lower 4 elements of 8 8-bit elements from each of two source
20 registers into 8 elements in a destination vector register.

Figure 9 illustrates shuffle operations for ordering 16-bit elements in a 64-bit doubleword.

Figure 10A illustrates a block diagram of a shuffle operation, which replicates the upper 2 elements of 4 16-bit elements from each of two source
25 registers into 4 elements in a destination vector register.

Figure 10B illustrates a block diagram of a shuffle operation, which replicates the lower 2 elements of 4 16-bit elements from each of two source registers into 4 elements in a destination vector register.

5 Figure 10C illustrates a block diagram of a shuffle operation, which replicates 2 odd elements of 4 16-bit elements from each of two source registers into 4 elements in a destination vector register.

Figure 10D illustrates a block diagram of a shuffle operation, which replicates 2 even elements of 4 16-bit elements from each of two source registers into 4 elements in a destination vector register.

10 Figure 10E illustrates a block diagram of a shuffle operation, which replicates even elements 0 and 2 from one source register into odd elements 1 and 3 in a destination vector register and further replicates odd elements 1 and 3 from another source register into the even elements 0 and 2, respectively, of the destination vector register.

15 Figure 10F illustrates a block diagram of a shuffle operation, which replicates even elements 0 and 2 from one source register into odd elements 3 and 1, respectively, in a destination vector register and further replicates odd elements 1 and 3 from another source register into the even elements 2 and 0, respectively, of the destination vector register.

20 Figure 10G illustrates a block diagram of a shuffle operation, which replicates the upper 2 elements of 4 16-bit elements from each of two source registers into a destination vector register.

Figure 10H illustrates a block diagram of a shuffle operation, which replicates the lower 2 elements of 4 16-bit elements from each of two source
25 registers into a destination vector register.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one skilled in the art that the present invention may be practiced without these specific details. In other instances well known methods, procedures, components, and circuits have not been described in detail so as not to unnecessarily obscure aspects of the present invention.

10 The present invention, a method for providing alignment and ordering of vector elements for single-instruction multiple-data (SIMD) processing, is described. The preferred embodiment of the present invention provides elements aligned and ordered for an efficient SIMD vector operation in a processor having 64-bit wide datapath within an exemplary computer system described below. Although such a datapath is exemplified herein, the present invention can be readily adapted to suit other datapaths of varying widths.

COMPUTER SYSTEM ENVIRONMENT

20 Figure 2 illustrates an exemplary computer system 200 comprised of a system bus 206 for communicating information, a processor 202 coupled with the bus 206 for processing information and instructions, a computer readable volatile memory unit 210 (e.g., random access memory, static RAM, dynamic RAM, etc.) coupled with the bus 206 for storing information and instructions for the processor 202, a computer readable non-volatile memory unit 208 (e.g., read only memory, programmable ROM, flash memory, EPROM, EEPROM, etc.) coupled with the bus 206 for storing static information and instructions

for the processor 202. A vector register file 204 containing a plurality of registers is included in the processor 202. In the present invention, the term vector register file 204 encompasses any register file containing a plurality of registers and as such is not limited to vector register files.

5

The computer system 200 of Figure 2 further includes a mass storage computer readable data storage device 212 (hard drive, floppy, CD-ROM, optical drive, etc.) such as a magnetic or optical disk and disk drive coupled with the bus 206 for storing information and instructions. Optionally, the
10 computer system 200 may include a display device 214 coupled to the bus 206 for displaying information to the user, an alphanumeric input device 216 including alphanumeric and function keys coupled to the bus 206 for communicating information and command selections to the processor 202, a cursor control device 218 coupled to the bus 206 for communicating user
15 input information and command selections to the processor 202, and a signal generating device 220 coupled to the bus 206 for communicating command selections to the processor 202.

According to an exemplary embodiment of the present invention, the
20 processor 202 includes a SIMD vector unit that functions as a coprocessor for or as an extension of the processor 202. The SIMD vector unit performs various arithmetic and logical operations on each data element within a SIMD vector in parallel. The SIMD vector unit utilizes the register files of the processor 202 to hold SIMD vectors. The present invention may include one
25 or more SIMD vector units to perform specialized operations such as arithmetic operations, logical operations, etc.

Figure 3 illustrates a block diagram of an exemplary datapath 300 for aligning and ordering vector elements. The datapath 300 includes a SIMD vector unit 302, an alignment unit 322, a register file 304, a crossbar circuit 314, and a vector load/store unit 302. The vector load/store unit 302 performs

5 load and store functions. It loads a vector from memory into one of the registers in the register file 304. It also stores a vector from one of the registers in the register file 304 into main memory. The alignment unit 312 receives two vectors from two source registers such as vs 306 and vt 308. Then, the alignment unit 312 extracts an aligned vector from the two vectors and stores

10 it into a destination register such as vd 310. The crossbar circuit 314 also receives two vectors two exemplary source registers, vs 306 and vt 308. The crossbar circuit 314 then selects a set of elements from the source registers and routes each of the elements in the selected set to a specified element in the exemplary destination register, vd 310. In an alternative embodiment, the

15 crossbar circuit 314 may receive one vector from a single source register and select a set of elements from the vector. The data path 318 allows a result to be forwarded to the register file 304 or to the vector load/store unit to be stored into main memory.

20 The SIMD vector unit 302 represents a generic SIMD vector processing unit, which may be an arithmetic unit, logical unit, integer unit, etc. The SIMD vector unit 302 may receive either one or two vectors from one or two source registers. It should be appreciated that the present invention may include more than one SIMD vector unit performing various functions. The

25 SIMD vector unit 302 may execute an operation specified in the instruction on each element within a vector in parallel.

The exemplary vector register file 304 is preferably comprised of 32 64-bit general purpose registers. To this end, the preferred embodiment of the present invention utilizes the floating point registers (FGR) of a floating point unit (FPU) in the processor as its vector registers. In this shared arrangement, data is moved between the vector register file 304 and a memory unit through the vector load/store unit 302. These load and store operations are unformatted. That is, no format conversions are performed and therefore no floating-point exceptions can occur due to these operations. Similarly, data is moved between the vector register file 304 and the alignment unit 312, the crossbar circuit 314, or the SIMD vector unit 316 without format conversions, and thus no floating-point exception occurs.

The present invention allows data types of 8-, 16-bit, 32-, or 64-bit fields. Hence, a 64-bit doubleword vector may contain 8 8-bit elements, 4 16-bit elements, 2 32-bit elements, or 1 64-bit element. According to this convention, vector registers of the present invention are interpreted in the following data formats: Quad Half (QH), Oct Byte (OB), Bi word (BW), and Long (L). In QH format, a vector register is interpreted as having 16-bit elements. For example, a 64-bit vector register is interpreted as a vector of 4 signed 16-bit integers. OB format interprets a vector register as being comprised of 8-bit elements. Hence, an exemplary 64-bit vector register is seen as a vector of 8 unsigned 8-bit integers. In BW format, a vector register is interpreted as having 2 32-bit elements. L format interprets a vector register as having a 64-bit element. These data types are provided to be adaptable to various register sizes of a processor. As described above, data format conversion is not necessary between these formats and floating-point format.

According to a preferred embodiment of the present invention, exemplary source registers, vs and vt, are each used to hold a set of vector elements. A third exemplary vector register, vd, is created from the source registers and holds a set of elements selected from the source registers.

- 5 Although the registers, vs, vt, and vd, are used to associate vector registers with a set of vector elements, other vector registers are equally suitable for present invention.

LOAD/STORE INSTRUCTIONS

- 10 The load and store instructions of the present invention use a special load/store unit to load and store a 64-bit doubleword between a register in a register file such as an FPR and a memory unit. The doubleword is loaded through an exemplary load/store unit 302 illustrated above in Figure 3. The load/store unit performs loading or storing of a doubleword with upper 61
15 bits of an effective address. The lowest 3 bits specify a byte address within the 64-bit doubleword for alignment.

- According to a preferred embodiment, an effective address is formed by adding the contents of an index value in a general purpose register (GPR) to a
20 base address in another GPR. The effective address is doubleword aligned. During the loading process, the last three bits of the effective address are ignored by treating these bits as 0s. Hence, the effective address is comprised of bits 3 to 63. The three bits from 0 to 2 contain the byte address for accessing individual bytes within a doubleword and are ignored by treating the three
25 bits as 0s. If the size of a register in a register file is 64-bits, then the 64-bit data stored in memory at the effective address is fetched and loaded into the register. If on the other hand, the size of the register in the register file is 32-

bits, then the lower 32 bits of the data are loaded into the vector register and the upper 32 bits of the data are loaded into the next register in sequence. Hence, a pair of 32-bit registers are used to hold a 64-bit data from the memory.

5

Conversely, the store instruction stores a doubleword from a vector register such as an FPR to the memory while ignoring alignment. The store operation is carried out through the exemplary load/store unit 302 illustrated above in Figure 3. The contents of a 64-bit doubleword in FPR, *fs*, is stored at the memory location specified by the effective address. The contents of GPR index and GPR base are added to form the effective address. The effective address is doubleword aligned. The last three bits of the effective address are ignored.

15 The effective address is formed by adding the contents of an index value in a general purpose register (GPR) to a base address in another GPR while ignoring the lowest three bits of the effective address by interpreting them as 0s. That is, the effective address is comprised of bits 3 to 63. The ignored three bits contain the byte address for accessing individual bytes within a doubleword. If the size of a vector register is 64-bits, then the content of the vector register is stored into memory. If on the other hand, the size of a vector register is 32-bits, then the lower 32 bits of the data are concatenated with the upper 32 bits of the data contained in the next register in sequence. Then, the concatenated 64-bit doubleword is stored into memory at the address specified by the effective address.

25

ALIGNMENT INSTRUCTION

The present alignment instruction operates on two 64-bit doublewords loaded into two registers from memory by issuing two load instructions. One doubleword is loaded into a first register (vs) and the other doubleword is
5 loaded into a second register (vt). The alignment instruction generates a 64-bit doubleword vector in a third register (vd) aligned for a SIMD vector operation. Preferably, an alignment unit performs alignment of a vector by funnel shift to extract an aligned 64-bit vector of elements from the two 64-bit registers.

10

Figure 4 illustrates a block diagram of an alignment unit in a processor for aligning a vector of elements. The vector load/store unit 404 loads two vectors from main memory 402 into two vector registers, vs and vt, in a register file 408. The alignment unit 410 receives the two vectors in the
15 vector registers, vs and vt, and extracts a byte aligned vector. Three control lines 412 representing three bits for the byte address controls the byte alignment performed through the alignment unit 410. The aligned vector is then forwarded to an exemplary vector register, vd, in the register file.

20 The alignment of a vector is dependent on a byte ordering mode of a processor. Byte ordering within a larger data size such as a 64-bit doubleword may be configured in either big-endian or little-endian order. Endian order refers to the location of byte 0 within a multi-byte data. A processor according to the present invention may be configured as either a big-endian or little-
25 endian system. For example, in a little-endian system, byte 0 is the least significant (i.e., rightmost) byte. On the other hand, in a big-endian system, byte 0 is the most significant (i.e., leftmost) byte. In the present invention, an

exemplary processor uses byte addressing for a doubleword access, which is aligned on a byte boundary divisible by eight (i.e., 0, 8, 16, ..., 56). Hence, a 64-bit doubleword loaded into a register in a processor is byte-aligned in either a big-endian or a little-endian mode. For a little-endian mode processor, the starting (i.e., first) byte for a vector to be extracted lies in the second vector register. Conversely for a big-endian mode processor, the starting (i.e., first) byte for the vector resides in the first vector register.

Figure 5 illustrates a flow diagram of the steps involved in extracting an aligned vector from two exemplary vectors. In step 502, two 64-bit doublewords are loaded from a memory unit into two 64-bit registers. One 64-bit doubleword is loaded into a first register and the other 64-bit doubleword in memory is loaded into the second register. Preferably, the former doubleword and the next doubleword are stored in contiguous memory space and their starting addresses differ by 64-bits or 8 bytes. The loading of the doublewords are accomplished through a load/store unit according to the load instruction described above.

The starting byte address of the aligned vector to be extracted is then determined in step 704. According to the preferred embodiment, the register and vector are all 64-bit wide. Since a 64-bit doubleword contains 8 bytes, three bits are needed to specify all the byte positions in a 64-bit doubleword. Hence, the preferred embodiment uses 3 bits to specify the position of the starting byte address in a 64-bit vector.

In one embodiment of the present invention, an alignment instruction provides an immediate, which is a constant byte address within a

doubleword. Preferably, the immediate consists of 3 bits for specifying a constant byte address to a byte among 8 bytes each in the first register (i.e., little-endian mode processor) and the second register (i.e., bit-endian mode processor). This alignment instruction performs a constant alignment of a
5 vector. The align amount is computed by masking the immediate, then using that value to control a funnel shift of vector vs concatenated with vector vt. The operands can be in the QH, OB, or BW format.

In an alternative embodiment, the alignment instruction provides a
10 variable byte addressing by specifying an address of a general purpose register (GPR) containing the starting byte address in the first register. This instruction accesses the GPR by using the address provided in the alignment instruction. Then, the instruction extracts the lower 3 bits in the GPR to obtain the starting byte address in the first register (i.e., little-endian mode) or
15 the second register (i.e., big-endian mode). The align amount is computed by masking the contents of GPR, rs, then using that value to control a funnel shift of vector vs concatenated with vector vt. The operands can be in QH, OB, or BW format.

20 After determining the starting byte address in step 504 of the flowchart in Figure 5, the first bit of the starting byte address is determined in step 506 by multiplying the starting byte address by 8. For example, if the starting byte address were 3, the first bit of the starting byte address is $3*8$ or 24. Then in step 508, a 64-bit doubleword is extracted by concatenating from the first bit at
25 the starting byte address in one register continuing through the other register. This concatenation is accomplished by funnel shifting from the first bit of the starting byte. Specifically, the first register is assigned bit positions from 0 to

63. The second register is assigned the next 64 bit positions from 64 to 127. The extraction scheme depends on the byte ordering modes. A variable s , representing the first bit position at the starting byte address, can be used to simplify the illustration of the differences between the byte ordering modes.
- 5 In a big-endian byte mode, the concatenation occurs from bit position $127-s$ to $64-s$. Conversely, in a little-endian byte mode, the concatenation occurs from bit position s through $63+s$.

Then in step 510, the extracted vector is replicated into a destination register in the register file for SIMD vector processing. In an alternative, embodiment, the extracted vector may be stored into the memory unit for later use. The process then terminates in step 512.

SHUFFLE INSTRUCTION

- 15 The shuffle instruction according to the present invention provides a vector of ordered elements selected from either one or two other vector registers. One or more load/store instructions are used to load the vector(s) into registers for shuffle operation. One embodiment uses a full byte-mode crossbar to generate a vector of elements selected from the elements of two
- 20 other exemplary vectors. That is, selected elements of the exemplary vectors, vs and vt , are merged into a new exemplary vector, vd . The new vector, vd , contains elements aligned for SIMD operation. Alternatively, a plurality of shuffle operations may be carried out to arrange the elements in a desired order for SIMD vector processing.

25

Figure 6A illustrates a block diagram of a full byte-mode crossbar circuit 600 used in generating a vector of elements from elements of two registers.

First, two vectors from a memory unit are loaded into two exemplary registers in a processor; the elements of the first vector are loaded into the first register, vs 602, and the elements of the second vector are loaded into the second register, vt 604. The elements of these two vector registers, vs 602 and
5 vt 604, serve as source elements. The crossbar circuit 600 receives as input each of the elements from the two vector registers in parallel. A set of control lines 608 is coupled to the crossbar circuit 600 to relay a specific shuffle instruction operation. The shuffle instruction operation encodes a destination element for each of the selected source elements. In response to
10 the specific shuffle instruction operation signals, the crossbar circuit 600 selects a set of elements from the two registers, vs 602 and vt 604, and routes or replicates each element to its associated destination element in an exemplary destination register, vd 606.

15 In addition, the present invention allows zeroing and sign extension of elements. For example with reference to Figure 6A, the present invention provides either zeroing or sign extension for each element in the first register, vs 602. In addition to providing the entire bits to the crossbar circuit 600, elements 0 through 7 in the first register, vs 602, provides their corresponding
20 sign bits 612, 614, 616, 618, 620, 622, 624, and 626 (612 through 626) to the associated AND gates 628, 630, 632, 634, 636, 638, 640, and 642 (628 through 642). Each of the AND gates 628 through 642 also receives as the other input, a control signal 610, which originate from a specific shuffle instruction for specifying either zeroing or sign extension mode.

25

Figure 6B shows a more detailed diagram of the operation of the exemplary AND gate 628 associated with element 7 in the first register, vs 602.

The AND gate 628 receives a single sign bit 612 from the most significant bit in the element 7 of the first register, vs 602. The AND gate 628 also receives the control signal 610. To provide zeroing for element 7 for example, the control signal 610 inputs a 0 into the AND gate 628. In this case, the output
5 652 at the AND gate 628 is 0 no matter what the input is at the sign bit 612. On the other hand, when the control signal is 1, the AND gate 628 generates the sign bit 612 as the output 652, whatever the sign is. In both cases of zeroing and sign extension, the output 652 is routed to a plurality of output lines 654 for replicating the output signal into an appropriate width. Preferably, the
10 output lines 654 matches the number of bits in each element in the first register, vs 602. The crossbar circuit 600 accepts the signals on these output lines 652 and uses these signals to zero or sign extend element 7 when necessary according to a shuffle instruction. The AND gates for the other elements 0 to 6 operate in a similar manner to provide zeroing and sign
15 extension bit signals to the crossbar circuit 600.

The preferred embodiment of the present invention operates on vectors of elements in a preferred OB or QH mode. In an OB mode, a 64-bit doubleword vector is interpreted as having 8 8-bit elements. In a QH mode,
20 the 64-bit vector is treated as containing 4 16-bit elements. For example, in OB mode, the crossbar circuit 600 selects, in parallel, as source elements eight 8-bit elements among the elements in the registers vs 602 and vt 604. Each of the eight elements is then replicated or routed into a particular destination element in the destination vector register, vd 606. In QH mode, the crossbar
25 circuit selects four 16-bit elements and replicates or routes each element into a particular destination element in the destination register. Those skilled in the art will appreciate that the crossbar circuit represents one embodiment of

the present invention in implementing the shuffle instruction operations. A crossbar circuit is well known the art and is commonly used in conjunction with vector processing units.

5 Figure 7 illustrates shuffle operations for ordering 8-bit elements in a 64-bit doubleword. Each row represents the destination vector register, vd, comprised of 8 elements, vd[0] to vd[7]. The first row 702 is comprised of placeholders to indicate the 8 elements. Below the first row 702 are 8 different shuffle operations in OB mode as indicated by the content of destination
10 vector register, vd, for each row 704 to 718. These shuffle operations in OB mode are illustrated in Figures 8A through 8H.

Figure 8A illustrates a block diagram of a shuffle operation, which converts four unsigned upper bytes (i.e., 8 bits) in a source register to four 16-
15 bit halves in a destination register. This shuffle operation, represented by mnemonic UPUH.OB, selects the upper 4 8-bit elements in an exemplary vector register, vs. The selected elements vs[4], vs[5], vs[6], and vs[7] are replicated into destination elements vd[0], vd[2], vd[4], and vd[6], respectively. The odd elements of the destination vector register vd[1], vd[3], vd[5], and
20 vd[7] are zeroed.

Figure 8B illustrates a block diagram of a shuffle operation, which converts a vector of unsigned low 4 bytes in a register to 16-bit halves. This shuffle operation, represented by mnemonic UPUL.OB, selects the lower 4 8-
25 bit elements in an exemplary vector register, vs. The selected elements vs[0], vs[1], vs[2], and vs[3] are replicated into destination elements vd[0], vd[2],

vd[4], and vd[6], respectively. The odd elements of the destination vector register vd[1], vd[3], vd[5], and vd[7] are zeroed.

Figure 8C illustrates a block diagram of a shuffle operation, which
5 converts a vector of signed upper 4 bytes in a register to 16-bit halves. This shuffle operation, represented by mnemonic UPSH.OB, selects the upper 4 8-bit elements in an exemplary vector register, vs. The selected elements vs[4], vs[5], vs[6], and vs[7] are replicated into destination elements vd[0], vd[2], vd[4], and vd[6], respectively. The odd elements of the destination vector
10 register vd[1], vd[3], vd[5], and vd[7] replicates the sign bits of the selected elements vs[4], vs[5], vs[6], and vs[7], respectively.

Figure 8D illustrates a block diagram of a shuffle operation, which
converts a vector of signed low 4 bytes in a register to 16-bit halves. This
15 shuffle operation, represented by mnemonic UPSL.OB, selects the lower 4 8-bit elements in an exemplary vector register, vs. The selected elements vs[0], vs[1], vs[2], and vs[3] are replicated into destination elements vd[0], vd[2], vd[4], and vd[6], respectively. The odd elements of the destination vector register vd[1], vd[3], vd[5], and vd[7] replicates the sign bits of the selected
20 elements vs[0], vs[1], vs[2], and vs[3], respectively.

Figure 8E illustrates a block diagram of a shuffle operation, which
replicates the odd elements of 8 8-bit elements from each of two source registers into 8 elements in a destination vector register. This shuffle
25 operation, represented by an exemplary mnemonic PACH.OB, selects the odd elements of 8 8-bit elements in exemplary source vector registers, vs and vt. The elements selected from vs, namely vs[1], vs[3], vs[5], and vs[7] are

replicated into destination elements vd[4], vd[5], vd[6], and vd[7], respectively. The elements vt[1], vt[3], vt[5], and vt[7] from the vector register vt are replicated into destination elements vd[0], vd[1], vd[2], and vd[3], respectively.

- 5 Figure 8F illustrates a block diagram of a shuffle operation, which replicates the even elements of 8 8-bit elements from each of two source registers into 8 elements in a destination vector register. This shuffle operation, represented by an exemplary mnemonic PACL.OB, selects the even elements of 8 8-bit elements in exemplary source vector registers, vs and vt.
- 10 The elements selected from vs, namely vs[0], vs[2], vs[4], and vs[8] are replicated into destination elements vd[4], vd[5], vd[6], and vd[7], respectively. The elements vt[0], vt[2], vt[4], and vt[6] from the vector register vt are replicated into destination elements vd[0], vd[1], vd[2], and vd[3], respectively.

- 15 Figure 8G illustrates a block diagram of a shuffle operation, which replicates the upper 4 elements of 8 8-bit elements from each of two source registers into 8 elements in a destination vector register. This shuffle operation, represented by an exemplary mnemonic MIXH.OB, selects the upper 4 elements of 8 8-bit elements in exemplary source vector registers, vs
- 20 and vt. The elements selected from vs, namely vs[4], vs[5], vs[6], and vs[7] are replicated into the odd elements of the destination vector register, namely vd[1], vd[3], vd[5], and vd[7], respectively. The elements vt[4], vt[5], vt[6], and vt[7] from the vector register vt are replicated into the even elements of the destination elements vd[0], vd[2], vd[4], and vd[6], respectively.

25

Figure 8H illustrates a block diagram of a shuffle operation, which replicates the lower 4 elements of 8 8-bit elements from each of two source

registers into 8 elements in a destination vector register. This shuffle operation, represented by an exemplary mnemonic MIXL.OB, selects the lower 4 elements of 8 8-bit elements in exemplary source vector registers, vs and vt. The elements selected from vs, namely vs[0], vs[1], vs[2], and vs[3] are replicated into the odd elements of the destination vector register, namely
5 vd[1], vd[3], vd[5], and vd[7], respectively. The elements vt[0], vt[1], vt[2], and vt[3] from the vector register vt are replicated into the even elements of the destination elements vd[0], vd[2], vd[4], and vd[6], respectively.

10 A shuffle instruction operating in QH mode generates a new vector of elements for two types of operations. The first type of operation creates a vector of new data sizes by converting data sizes between 16-bit elements and 32-bit elements in a vector. The second type creates a new vector of elements drawn from two other vectors. The present exemplary data type conversion
15 operations enable a larger range of computational data format than their storage format, such as 32 bit computation on 16 bit numbers. In addition, the present embodiment operations allow conversion of a data set from a smaller range format to a larger range format or vice versa as between 16 and 32 bit data.

20

Figure 9 illustrates shuffle operations for ordering 16-bit elements in a 64-bit doubleword. Each row represents the destination vector register, vd, comprised of 4 elements, vd[0] to vd[7]. The first row 902 is comprised of placeholders to indicate the 4 elements. Below the first row 902 are 4 different
25 shuffle operations in QH mode as indicated by the content of destination vector register, vd, for each row 904 to 918. These shuffle operations in QH mode are illustrated in Figures 10A through 10H.

Figure 10A illustrates a block diagram of a shuffle operation, which replicates the upper 2 elements of 4 16-bit elements from each of two source registers into 4 elements in a destination vector register. This shuffle operation, represented by an exemplary mnemonic MIXH.QH, selects the upper 2 elements of 4 16-bit elements in exemplary source vector registers, vs and vt. The elements selected from vs, namely vs[2] and vs[3] are replicated into the odd elements of the destination vector register, namely vd[1] and vd[3], respectively. The elements vt[2] and vt[3] from the vector register vt are replicated into the even elements of the destination elements vd[0] and vd[2], respectively.

Figure 10B illustrates a block diagram of a shuffle operation, which replicates the lower 2 elements of 4 16-bit elements from each of two source registers into 4 elements in a destination vector register. This shuffle operation, represented by an exemplary mnemonic MIXL.QH, selects the lower 2 elements of 4 16-bit elements in exemplary source vector registers, vs and vt. The elements selected from vs, namely vs[0] and vs[1] are replicated into the odd elements of the destination vector register, namely vd[1] and vd[3], respectively. The elements vt[0] and vt[1] from the vector register vt are replicated into the even elements of the destination elements vd[0] and vd[2], respectively.

Figure 10C illustrates a block diagram of a shuffle operation, which replicates 2 odd elements of 4 16-bit elements from each of two source registers into 4 elements in a destination vector register. This shuffle operation, represented by an exemplary mnemonic PACH.QH, selects the 2

odd elements of 4 16-bit elements in exemplary source vector registers, vs and vt. The elements selected from vs, namely vs[1] and vs[3] are replicated into the upper 2 elements of the destination vector register, namely vd[2] and vd[3], respectively. The elements vt[1] and vt[3] from the vector register vt are
5 replicated into the lower 2 elements of the destination elements vd[0] and vd[1], respectively.

Figure 10D illustrates a block diagram of a shuffle operation, which replicates 2 even elements of 4 16-bit elements from each of two source registers into 4 elements in a destination vector register. This shuffle
10 operation, represented by an exemplary mnemonic PACL.QH, selects the 2 even elements of 4 16-bit elements in exemplary source vector registers, vs and vt. The elements selected from vs, namely vs[0] and vs[2] are replicated into the upper 2 elements of the destination vector register, namely vd[2] and
15 vd[3], respectively. The elements vt[0] and vt[2] from the vector register vt are replicated into the lower 2 elements of the destination elements vd[0] and vd[1], respectively.

Figure 10E illustrates a block diagram of a shuffle operation, which
20 replicates even elements from one source register and odd elements from another source register into a destination vector register. This shuffle operation, represented by an exemplary mnemonic BFLA.QH, selects the 2 even elements of 4 16-bit elements from an exemplary source vector register, vs. The shuffle operation also selects the 2 odd elements of 4 16-bit elements
25 from another exemplary source vector register, vt. The even elements selected from vs, namely vs[0] and vs[2] are replicated into the 2 odd elements of the destination vector register, namely vd[1] and vd[3], respectively. The

odd elements $vt[1]$ and $vt[3]$ from the vector register vt are replicated into the 2 even elements of the destination elements $vd[0]$ and $vd[1]$, respectively.

Figure 10F illustrates a block diagram of a shuffle operation, which
5 replicates even elements from one source register and odd elements from
another source register into a destination vector register. This shuffle
operation, represented by an exemplary mnemonic BFLB.QH, selects the 2
even elements of 4 16-bit elements from an exemplary source vector register,
 vs . The shuffle operation also selects the 2 odd elements of 4 16-bit elements
10 from another exemplary source vector register, vt . The even elements
selected from vs , namely $vs[0]$ and $vs[2]$ are replicated into the 2 odd elements
of the destination vector register in reverse order, namely $vd[3]$ and $vd[1]$,
respectively. The odd elements $vt[1]$ and $vt[3]$ from the vector register vt are
replicated into the 2 even elements of the destination elements in reverse
15 order, namely $vd[0]$ and $vd[1]$, respectively.

Figure 10G illustrates a block diagram of a shuffle operation, which
replicates the upper 2 elements of 4 16-bit elements from each of two source
registers into a destination vector register. This shuffle operation,
20 represented by an exemplary mnemonic REPA.QH, selects the upper 2
elements of 4 16-bit elements in exemplary source vector registers, vs and vt .
The upper elements selected from vs , namely $vs[2]$ and $vs[3]$ are replicated
into the upper elements of the destination vector register, namely $vd[2]$ and
 $vd[3]$, respectively. The upper elements $vt[2]$ and $vt[3]$ from the vector register
25 vt are replicated into the lower elements of the destination elements $vd[0]$
and $vd[1]$, respectively.

Figure 10H illustrates a block diagram of a shuffle operation, which replicates the lower 2 elements of 4 16-bit elements from each of two source registers into a destination vector register. This shuffle operation, represented by an exemplary mnemonic `REPB.QH`, selects the lower 2
5 elements of 4 16-bit elements in exemplary source vector registers, `vs` and `vt`. The lower elements selected from `vs`, namely `vs[0]` and `vs[1]` are replicated into the upper elements of the destination vector register, namely `vd[2]` and `vd[3]`, respectively. The lower elements `vt[0]` and `vt[1]` from the vector register `vt` are replicated into the lower elements of the destination elements `vd[0]`
10 and `vd[2]`, respectively.

The shuffle instructions allow more efficient SIMD vector operations. First, the shuffle operation creates a vector of new data sizes by converting between 8-bit elements and 16-bit elements in a vector. These data type
15 conversions enable a larger range of computational data format than their storage format, such as 16 bit computation on 8 bit numbers. For example, these operations allow conversion of a data set from a smaller range format to a larger range format or vice versa as between 8 and 16 bit audio or video data.

20

Second, the shuffle operations are also useful in interleaving and deinterleaving data. For example, some applications store multiple channel data in separate arrays, or interleaved in a single array. These applications typically require interleaving or deinterleaving the multiple channels. In
25 these applications, separate R, G, B, A byte arrays may be converted into an interleaved RGBA array by the following series of shuffle instructions:

```
MIXL.OB RGL, R, G          ; RGRGRGRG
```

```

MIXL.OB BAL, B, A      ; BABABABA
MIXH.OB RGH, R, G      ; RGRGRGRG
MIXH.OB BAH, B, A      ; BABABABA
MIXL.QS RGBALL, RGL, BAL ; RGBARGBA
5 MIXH.QS RGBALH, RGL, BAL ; RGBARGBA
MIXL.QS RGBAHL, RGH, BAH ; RGBARGBA
MIXH.QS RGBAHH, RGH, BAH ; RGBARGBA

```

Conversely, an interleaved RGBA array may be deinterleaved into separate R, G, B, and A arrays by the following series of shuffle instructions:

```

10 PACL.OB GA0GA1, RGBA0, RGBA1
PACH.OB RB0RB1, RGBA0, RGBA1
PACL.OB GA2GA3, RGBA2, RGBA3
PACH.OB RB2RB3, RGBA2, RGBA3
15 PACL.OB A0A1A2A3, GA0GA1, GA2GA3
PACH.OB G0G1G2G3, GA0GA1, GA2GA3
PACL.OB B0B1B2B3, RB0RB1, RB2RB3
PACH.OB R0R1R2R3, RB0RB1, RB2RB3

```

20 Third, some algorithms operate on 2 dimensional arrays of data such as images. Such an array typically orders the elements of the array in a major axis, where the elements are consecutive, and a minor axis, where the elements are separated by the size of the major axis. Often, a transpose operation is performed on the 2 dimensional array by converting the major

25 axis to minor axis and vice versa. A common example is a discrete cosine transformation (DCT) requiring transposing 8x8 block of array. In this example, the 8x8 block of array consists of following elements:

		d0	d1	d2	d3	d4	d5	d6	d7
30	s0	A0	B0	C0	D0	E0	F0	G0	H0
	s1	A1	B1	C1	D1	E1	F1	G1	H1
	s2	A2	B2	C2	D2	E2	F2	G2	H2
	s3	A3	B3	C3	D3	E3	F3	G3	H3
	s4	A4	B4	C4	D4	E4	F4	G4	H4
35	s5	A5	B5	C5	D5	E5	F5	G5	H5
	s6	A6	B6	C6	D6	E6	F6	G6	H6
	s7	A7	B7	C7	D7	E7	F7	G7	H7

The present invention can transpose the 8x8 transpose in OB mode in 24 instructions, of which 12 are shown as follows:

5	MIXH.OB t0, s0, s1	A0 A1 B0 B1 C0 C1 D0 D1
	MIXH.OB t1, s2, s3	A2 A3 B2 B3 C2 C3 D2 D3
	MIXH.OB t2, s4, s5	A4 A5 B4 B5 C4 C5 D4 D5
	MIXH.OB t3, s6, s7	A6 A7 B6 B7 C6 C7 D6 D7
	MIXH.QH u0, t0, t1	A0 A1 A2 A3 B0 B1 B2 B3
	MIXH.QH u1, t2, t3	A4 A5 A6 A7 B4 B5 B6 B7
10	MIXH.QH u2, t0, t1	C0 C1 C2 C3 D0 D1 D2 D3
	MIXH.QH u3, t2, t3	C4 C5 C6 C7 D4 D5 D6 D7
	REPA.QH d0, u0, u1	A0 A1 A2 A3 A4 A5 A6 A7
	REPB.QH d1, u0, u1	B0 B1 B2 B3 B4 B5 B6 B7
	REPA.QH d2, u2, u3	C0 C1 C2 C3 C4 C5 C6 C7
15	REPB.QH d3, u2, u3	D0 D1 D2 D3 D4 D5 D6 D7
	MIXL.OB t0, s0, s1	E0 E1 F0 F1 G0 G1 H0 H1
	MIXL.OB t1, s2, s3	E2 E3 F2 F3 G2 G3 H2 H3
	MIXL.OB t2, s4, s5	E4 E5 F4 F5 G4 G5 H4 H5
20	MIXL.OB t3, s6, s7	E6 E7 F6 F7 G6 G7 H6 H7
	MIXL.QH u0, t0, t1	E0 E1 E2 E3 F0 F1 F2 F3
	MIXL.QH u1, t2, t3	E4 E5 E6 E7 F4 F5 F6 F7
	MIXL.QH u2, t0, t1	G0 G1 G2 G3 H0 H1 H2 H3
	MIXL.QH u3, t2, t3	G4 G5 G6 G7 H4 H5 H6 H7
25	REPA.QH d0, u0, u1	E0 E1 E2 E3 E4 E5 E6 E7
	REPB.QH d1, u0, u1	F0 F1 F2 F3 F4 F5 F6 F7
	REPA.QH d2, u2, u3	G0 G1 G2 G3 G4 G5 G6 G7
	REPB.QH d3, u2, u3	H0 H1 H2 H3 H4 H5 H6 H7

30 In another example, an exemplary 4x4 array block consists of following elements:

		d0	d1	d2	d3
35	s0	A	B	C	D
	s1	E	F	G	H
	s2	I	J	K	L
	s3	M	N	O	P

A transpose operation of the 4x4 array block in QH mode uses 8 shuffle instructions as follows:

40	MIXH.QH t0, s0, s1	A E B F
	MIXH.QH t1, s2, s3	I M J N

	REPA.QH d0, t0, t1	A E I M
	REPB.QH d1, t0, t1	B F J N
5	MIXL.QH t0, s0, s1	C G D H
	MIXL.QH t1, s2, s3	K O L P
	REPA.QH d2, t0, t1	C G K O
	REPB.QH d3, t0, t1	D H L P

The shuffle instructions such as BFLA and BFLB allow reversing the order of elements in an array, in pairs or groups of 4. Larger groups can be reordered by memory or register address because they are a multiple of 64 bit elements. Inverting the order of a large array can be accomplished by inverting each vector of 4 elements with BFLB and loading from or storing each doubleword to the mirrored address in the array. Similarly, a butterfly on a large array can be assembled from double word addressing and BFLA or BFLB operations on the addressed doublewords.

The present invention thus provides a method for providing element alignment and ordering for SIMD processing. While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not be construed as being limited by such embodiments, but rather construed according to the claims below.

CLAIMS

What is claimed is:

1. In a computer system including a processor having a plurality of registers, a method for generating an aligned vector of first width from two
5 second width vectors for single instruction multiple data (SIMD) processing, comprising the steps of:
loading a first vector from a memory unit into a first register, wherein the first vector contains a first byte of an aligned vector to be generated;
loading a second vector from the memory unit into a second register;
10 determining a starting byte in the first register wherein the starting byte specifies the first byte of an aligned vector;
extracting a first width vector from the first register and the second register beginning from the first bit in the first byte of the first register continuing through the bits in the second register; and
15 replicating the extracted first width vector into a third register such that the third register contains a plurality of elements aligned for SIMD processing.
2. The method as recited in Claim 1 further comprising the step of
20 storing the aligned vector in the third register to the memory unit.
3. The method as recited in Claim 1, wherein the first width and second width are each 64 bits.
- 25 4. The method as recited in Claim 3, wherein the third register is comprised of 8 8-bit elements.

5. The method as recited in Claim 3, wherein the third register is comprised of 4 16-bit elements.

6. The method as recited in Claim 1, wherein the starting byte is
5 specified as a constant in an alignment instruction.

7. The method as recited in Claim 1, wherein the starting byte is specified as a variable in a register in an alignment instruction.

10 8. The method as recited in Claim 1, wherein the first vector and the second vector are in contiguous location in the memory unit.

9. The method as recited in Claim 1, wherein the processor operates in a big-endian byte ordering mode.
15

10. The method as recited in Claim 1, wherein the processor operates in a little-endian byte ordering mode.

11. In a computer system including a processor having a plurality of
20 registers, a method for generating an ordered set of elements in an N-bit vector from two sets of elements in two N-bit vectors for single instruction multiple data (SIMD) vector processing, said method comprising the steps of:
loading a first vector from a memory unit into a first register;
loading a second vector from the memory unit into a second register;
25 selecting a subset of elements from the first register and the second register; and
register; and

replicating the elements from the subset into the elements in the third register in a particular order suitable for subsequent SIMD vector processing.

12. The method as recited in Claim 11 further comprising the step of
5 storing the elements in the third register to the memory unit.

13. The method as recited in Claim 11, wherein the first vector and the second vector are each comprised of 4 16-bit elements indexed from 0 to 3.

10 14. The method as recited in Claim 11, wherein the first vector and the second vector are each comprised of 8 8-bit elements indexed from 0 to 7.

15 15. The method as recited in Claim 13, wherein the subset is comprised of two elements from the first register and two elements from the second register.

16. The method as recited in Claim 14, wherein the subset is comprised of four elements from the first register and four elements from the second register.

20

17. The method as recited in Claim 13, wherein the subset is comprised of the elements 2 and 3 from the first register and the elements 2 and 3 from the second register.

25 18. The method as recited in Claim 17, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 2 of the second register;

the element 1 replicated from the element 2 of the first register;
the element 2 replicated from the element 3 of the second register; and
the element 3 replicated from the element 3 of the first register.

5 19. The method as recited in Claim 13, wherein the subset is
 comprised of the elements 0 and 1 from the first register and the elements 0
 and 1 from the second register.

 20. The method as recited in Claim 19, wherein the particular order
10 of the elements in the third register comprises:

 the element 0 replicated from the element 0 of the second register;
 the element 1 replicated from the element 0 of the first register;
 the element 2 replicated from the element 1 of the second register; and
 the element 3 replicated from the element 1 of the first register.

15

 21. The method as recited in Claim 13, wherein the subset is
 comprised of the elements 1 and 3 from the first register and the elements 1
 and 3 from the second register.

20 22. The method as recited in Claim 21, wherein the particular order
 of the elements in the third register comprises:

 the element 0 replicated from the element 1 of the second register;
 the element 1 replicated from the element 3 of the second register;
 the element 2 replicated from the element 1 of the first register; and
25 the element 3 replicated from the element 3 of the first register.

23. The method as recited in Claim 13, wherein the subset is comprised of the elements 0 and 2 from the first register and the elements 0 and 2 from the second register.

5 24. The method as recited in Claim 23, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 0 of the second register;
the element 1 replicated from the element 2 of the second register;
the element 2 replicated from the element 0 of the first register; and
10 the element 3 replicated from the element 2 of the first register.

25. The method as recited in Claim 13, wherein the subset is comprised of the elements 0 and 2 from the first register and the elements 1 and 3 from the second register.

15

26. The method as recited in Claim 25, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 1 of the second register;
the element 1 replicated from the element 0 of the first register;
20 the element 2 replicated from the element 3 of the second register; and
the element 3 replicated from the element 2 of the first register.

27. The method as recited in Claim 13, wherein the subset is comprised of the elements 0 and 2 from the first register and the elements 1 and 3 from the second register.

25

28. The method as recited in Claim 27, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 3 of the second register;
the element 1 replicated from the element 2 of the first register;
5 the element 2 replicated from the element 1 of the second register; and
the element 3 replicated from the element 0 of the first register.

29. The method as recited in Claim 13, wherein the subset is comprised of the elements 2 and 3 from the first register and the elements 2
10 and 3 from the second register.

30. The method as recited in Claim 29, wherein particular order of the elements in the third register comprises:

the element 0 replicated from the element 2 of the second register;
15 the element 1 replicated from the element 3 of the second register;
the element 2 replicated from the element 2 of the first register; and
the element 3 replicated from the element 3 of the first register.

31. The method as recited in Claim 13, wherein the subset is comprised of the elements 0 and 2 from the first register and the elements 0
20 and 1 from the second register.

32. The method as recited in Claim 31, wherein the particular order of the elements in the third register comprises:

25 the element 0 replicated from the element 0 of the second register;
the element 1 replicated from the element 1 of the second register;
the element 2 replicated from the element 0 of the first register; and

the element 3 replicated from the element 2 of the first register.

33. The method as recited in Claim 14, wherein the subset is comprised of the elements 1, 3, 5, and 7 from the first register and the
5 elements 1, 3, 5, and 7 from the second register.

34. The method as recited in Claim 33, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 1 of the second register;
10 the element 1 replicated from the element 3 of the second register;
the element 2 replicated from the element 5 of the second register;
the element 3 replicated from the element 7 of the second register;
the element 4 replicated from the element 1 of the first register;
the element 5 replicated from the element 3 of the first register;
15 the element 6 replicated from the element 5 of the first register; and
the element 7 replicated from the element 7 of the first register.

35. The method as recited in Claim 14, wherein the subset is comprised of the elements 0, 2, 4, and 6 from the first register and the
20 elements 0, 2, 4, and 6 from the second register.

36. The method as recited in Claim 35, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 0 of the second register;
25 the element 1 replicated from the element 2 of the second register;
the element 2 replicated from the element 4 of the second register;
the element 3 replicated from the element 6 of the second register;

the element 4 replicated from the element 0 of the first register;
the element 5 replicated from the element 2 of the first register;
the element 6 replicated from the element 4 of the first register; and
the element 7 replicated from the element 6 of the first register.

5

37. The method as recited in Claim 14, wherein the subset is comprised of the elements 4, 5, 6, and 7 from the first register and the elements 4, 5, 6, and 7 from the second register.

10 38. The method as recited in Claim 37, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 4 of the second register;
the element 1 replicated from the element 4 of the first register;
the element 2 replicated from the element 5 of the second register;
15 the element 3 replicated from the element 5 of the first register;
the element 4 replicated from the element 6 of the second register;
the element 5 replicated from the element 6 of the first register;
the element 6 replicated from the element 7 of the second register; and
the element 7 replicated from the element 7 of the first register.

20

39. The method as recited in Claim 14, wherein the subset is comprised of the elements 0, 1, 2, and 3 from the first register and the elements 0, 1, 2, and 3 from the second register.

25 40. The method as recited in Claim 39, wherein the particular order of the elements in the third register comprises:

the element 0 replicated from the element 0 of the second register;

the element 1 replicated from the element 0 of the first register;
the element 2 replicated from the element 1 of the second register;
the element 3 replicated from the element 1 of the first register;
the element 4 replicated from the element 2 of the second register;
5 the element 5 replicated from the element 2 of the first register;
the element 6 replicated from the element 3 of the second register; and
the element 7 replicated from the element 3 of the first register.

41. The method as recited in Claim 14, wherein the subset is
10 comprised of the elements 4, 5, 6, and 7 from the first register.

42. The method as recited in Claim 41, wherein the particular order
of the elements in the third register comprises:
the element 0 replicated from the element 4 of the first register;
15 the element 2 replicated from the element 5 of the first register;
the element 4 replicated from the element 6 of the first register;
the element 6 replicated from the element 7 of the first register; and
the elements 1, 3, 5, and 7 containing a zero in all the bits.

20 43. The method as recited in Claim 14, wherein the subset is
comprised of the elements 0, 1, 2, and 3 from the first register.

44. The method as recited in Claim 43, wherein the particular order
of the elements in the third register comprises:
25 the element 0 replicated from the element 0 of the first register;
the element 2 replicated from the element 1 of the first register;
the element 4 replicated from the element 2 of the first register;

the element 6 replicated from the element 3 of the first register; and
the elements 1, 3, 5, and 7 containing a zero in all the bits.

45. The method as recited in Claim 14, wherein the subset is
5 comprised of the elements 4, 5, 6, and 7 from the first register.

46. The method as recited in Claim 45, wherein the particular order
of the elements in the third register comprises:
the element 0 replicated from the element 4 of the first register;
10 the element 1 replicating the sign bit of the element 4 of the first
register in all the bits;
the element 2 replicated from the element 5 of the first register;
the element 3 replicating the sign bit of the element 5 of the first
register in all the bits;
15 the element 4 replicated from the element 6 of the first register;
the element 5 containing the sign bit of the element 6 of the first
register in all the bits;
the element 6 replicated from the element 7 of the first register; and
the element 7 containing the sign bit of the element 7 of the first
20 register in all the bits.

47. The method as recited in Claim 14, wherein the subset is
comprised of the elements 0, 1, 2, and 3 from the first register.

25 48. The method as recited in Claim 47, wherein the particular order
of the elements in the third register comprises:
the element 0 replicated from the element 0 of the first register;

the element 1 containing the sign bits of the element 0 of the first
register;
the element 2 replicated from the element 1 of the first register;
the element 3 containing the sign bits of the element 1 of the first
5 register;
the element 4 replicated from the element 2 of the first register;
the element 5 containing the sign bits of the element 2 of the first
register;
the element 6 replicated from the element 3 of the first register; and
10 the element 7 containing the sign bits of the element 3 of the first
register.

ABSTRACT

The present invention provides alignment and ordering of vector elements for SIMD processing. In the alignment of vector elements for SIMD processing, one vector is loaded from a memory unit into a first register and
5 another vector is loaded from the memory unit into a second register. The first vector contains a first byte of an aligned vector to be generated. Then, a starting byte specifying the first byte of an aligned vector is determined. Next, a vector is extracted from the first register and the second register beginning from the first bit in the first byte of the first register continuing through the
10 bits in the second register. Finally, the extracted vector is replicated into a third register such that the third register contains a plurality of elements aligned for SIMD processing. In the ordering of vector elements for SIMD processing, a first vector is loaded from a memory unit into a first register and a second vector is loaded from the memory unit into a second register. Then,
15 a subset of elements are selected from the first register and the second register. The elements from the subset are then replicated into the elements in the third register in a particular order suitable for subsequent SIMD vector processing.

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☒ **BLACK BORDERS**
- ☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- ☐ **FADED TEXT OR DRAWING**
- ☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- ☒ **SKEWED/SLANTED IMAGES**
- ☐ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- ☐ **GRAY SCALE DOCUMENTS**
- ☒ **LINES OR MARKS ON ORIGINAL DOCUMENT**
- ☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- ☐ **OTHER:** _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.